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(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83716-9632 (US).

(72) Inventor: FARRAR, Paul, A.; 17 Yandow Drive, So. Burlington, VT 05403 (US).

(74) Agent: VIKSNINS, Ann, S.; Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).

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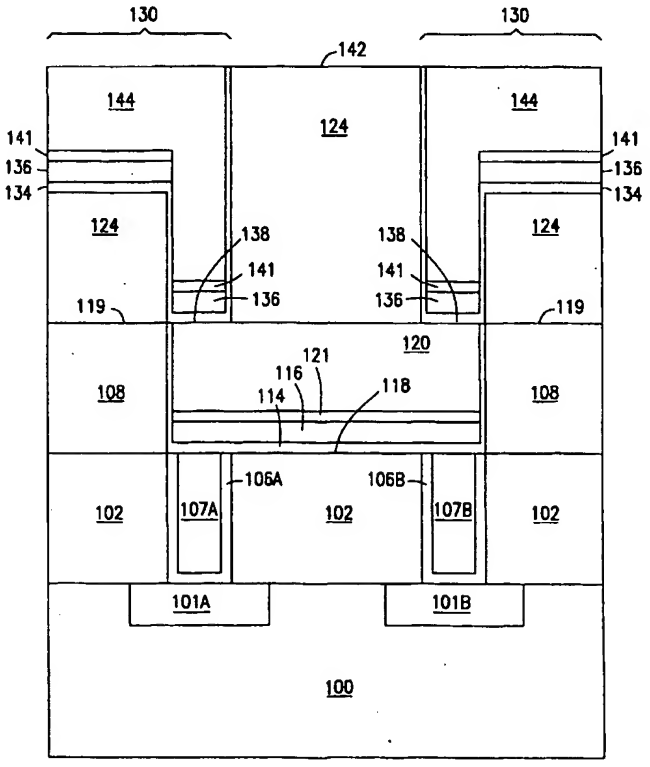

(57) Abstract: Structures and methods are provided which improve performance in integrated circuits. The structures and methods include a diffusion barrier (114) and a seed layer (116) in an integrated circuit both formed using a low energy ion implantation followed by a selective deposition of metal lines (120) for the integrated circuit. According to the teachings of the present invention, the selective deposition of the metal lines avoids the need for multiple chemical mechanical planarization (CMP) steps. The low energy ion implantation of the present invention allows for the distinct placement of both the diffusion barrier and the seed layer. A residual resist can be used to remove the diffusion barrier and the seed layer from unwanted areas on a wafer surface.

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PROCESS FOR PROVIDING SEED LAYERS FOR ALUMINUM, COPPER, GOLD AND SILVER METALLURGY

Related Applications

This application is related to the following co-filed and commonly assigned applications: attorney docket number 303.618US1, entitled "Method and Apparatus for Making Integrated-Circuit Wiring from Copper, Silver, Gold, and Other Metals," and attorney docket number 303.648US1, entitled "Method for Making Copper Interconnects in Integrated Circuits," which are hereby incorporated by reference. This application is further related to the following co-pending and commonly assigned application: U. S. Serial Number 09/128,859 filed August 9, 1999, (attorney docket number 303.473US1), entitled "Copper Metallurgy in Integrated Circuits," which is hereby incorporated by reference.

Field of the Invention

The present invention relates generally to integrated circuits. More particularly, it pertains to structures and methods for providing seed layers for integrated circuit metallurgy.

Background of the Invention

One of the main problems confronting the semiconductor processing industry, in the ULSI age, is that of Capacitive-Resistance loss in the wiring levels. This has led to a large effort to reduce the resistance of and lower the capacitive loading on the wiring levels. Since its beginning, the industry has relied on aluminum and aluminum alloys for wiring. In a like manner, the industry has mainly relied on SiO_2 as the insulator of choice, although polyimide was used in a number of products by one vendor (IBM), for a number of years. The capacitive resistance problem grows with each succeeding generation of technology. As the dimensions decrease the minimum line space combination decreases, thus increasing both capacitance and resistance, if the designer is to take advantage of the improved ground rules.

To improve the conductivity, it has been suggested by numerous investigators, that copper or perhaps silver or gold metallurgy be substituted for the aluminum metallurgy, now being used. Several potential problems have been encountered in the development of these proposed metallurgies. One of the

main ones is the fast diffusion of copper through both silicon and SiO_2. This along with the known junction poising effects of copper and gold have led to proposals to use a liner, to separate these metallurgies from the SiO_2 insulator.

For example, an article authored by Karen Holloway and Peter M. Fryer, entitled, "Tantalum as a diffusion barrier between copper and silicon", Appl. Phys. Letter vol.57, No. 17, 22 October 1990, pp. 1736-1738, suggests the use of a tantalum metal liner. In another article authored by T. Laursen and J. W. Mayer, entitled, "Encapsulation of Copper by Nitridation of Cu-Ti Alloy/Bilayer Structures", International Conference on Metallurgical Coatings and Thin Films, San Diego, CA, April 21-25, 1997, Abstract No. H1.03, pg. 309, suggests using a compound such as CuTi as the liner. Still another article published by Vee S.C. Len, R. E. Hurley, N. McCusker, D. W. McNill, B. M. Armstrong and H.S. Gamble, entitled, "An investigation into the performance of diffusion barrier materials against copper diffusion using metal-oxide-semiconductor (MOS) capacitor structures", Solid-State Electronics 43 (1999) pp. 1045-1049 suggests using a compound such as TaN as the liner. These approaches, however, do not fully resolve the above-stated problem of the minimum line space decreases. Thus, the shrinking line size in the metal line and liner combination again increases both the capacitance and resistance.

At the same time other investigators, in looking at the capacitive loading effect, have been studying various polymers such as fluorinated polyimides as possible substitutions for SiO_2 insulators. Several of these materials have dielectric constants considerably lower than SiO_2. However as in the case of SiO_2, an incompatibility problem with copper metallurgy has been found. For example, in a presentation by D. J. Godbey, L. J. Buckley, A. P. Purdy and A. W. Snow, entitled, "Copper Diffusion in Organic Polymer Resists and Inter-level Dielectrics", at the International Conference on Metallurgical Coatings and Thin Films, San Diego, CA, April 21-25, 1997, Abstract H2.04 pg. 313, it was shown that polyimide, and many other polymers, react with copper during the curing process, forming a conductive oxide CuO_2, which is dispersed within the polymer. This then raises the effective dielectric constant of the polymer and in many cases increases the polymers conductivity. In addition it has been found

that reactive ion etching (RIE) of all three metals, copper, silver or gold, is difficult at best.

Other approaches by investigators have continued to look for ways to continue to use aluminum wiring with a lower dielectric constant insulator. This would decrease the capacitive load with a given inter-line space but require wider or thicker lines. The use of thicker lines would increase the capacitive loading in direct proportion to the thickness increase. Thus to some measure, it defeats the objectives of decreasing the capacitive loading effects. Therefore, the use of thicker lines should be avoided as much as possible. As the resistivity of the line is directly proportional to its cross-sectional area, if it cannot be made thicker, it must be made wider. If however the lines are made wider, fewer wiring channels can be provided in each metal level. To obtain the same number of wiring channels, additional levels of metal must be provided. This increases the chip cost. So if this approach is to be followed, it is imperative that a low cost process sequence be adopted.

One approach provided by the present inventor in a co-pending application, entitled, "Copper Metallurgy in Integrated Circuits", filed August 4, 1998, application No. 09/128,859, proposes a method to solve many of the problems associated with using copper in a polymer insulator. This process, which was specifically designed to be compatible with a polymer or foam insulation, required that the unwanted copper on the surface of each layer be removed by Chemical Mechanical Polishing (CMP) or a similar planarizing process. However, this method may require careful process control, leading to additional expense. Another approach is provided in a co-pending application by Kie Ahn and Leonard Forbes, entitled "Method for Making Copper and Other Metal Interconnections in Integrated Circuits", filed February 27, 1998, U. S. Serial No. 09/032,197, which proposes a method using ionized sputtering to form the underlayer, then forming a low wetting layer on the areas where no copper is desired using jet vapor deposition. The copper is deposited with ionized Magnetron sputtering followed by hydrogen annealing. The excess copper is then removed by CMP as in the aforementioned application.

Another process is described by the present inventor in a co-pending application, entitled, "Integrated Circuit with Oxidation Resistant Polymeric

Layer", filed September 1, 1998, U. S. Serial No. 09/145,012, which eliminates many of the CMP processes and uses lift-off to define the trench and the seed layer simultaneously. A process is also described by the present inventor in a co-pending application, entitled, "Conductive Structures in Integrated Circuits" filed March 1, 1999, U. S. Serial No. 09/259,849, which required a CMP process to remove unwanted seed material prior to a selective deposition of the metal layers in a damascene or dual damascene process.

The use of CMP has proven to be effective in reducing local non-planarity. However, extensive dishing in wide lines and rounding of corners of the insulator are a common occurrence. It has been found that by maintaining a regular structure through the use of dummy structures and small feature sizes, it is possible to planarize a level to a nearly flat surface. The use of these techniques are however costly and in some cases come with density or performance penalties. It is, however, generally possible to planarize a structure prior to the metal levels using these methods with little or no density penalty. The use of electroless plating has been suggested in an article authored by Yosi Schacham-Diamand and Valery M. Dubin, entitled "Copper electroless deposition technology for ultra-large scale-integration (ULSI) metallization", Microelectronic Engineering 33 (1997) 47-58, however a simple process for obtaining both a barrier layer as well as a seed layer is needed to improve the cost effectiveness of this technique. One technique for seeding polyimide and silicon surfaces using high energy (10-20 Kilo Electron Volts {KEV}) ion implantation has been demonstrated in an article authored by S. Bhansali, D. K. Sood and R. B. Zmood, entitled "Selective electroless copper plating on silicon seeded by copper ion implantation", Thin Solid Films V253 (1994) pp. 391-394. However this process has not been shown to be implementable into a product structure where a barrier and/or adhesion layer is required.

For the reasons stated above and for others which will become apparent from reading the following disclosure, structures and methods are needed which alleviate the problems associated with via and metal line fabrication processes. These structures and methods for via and metal line fabrication must be streamlined and accommodate the demand for higher performance in integrated circuits even as the fabrication design rules shrink.

Summary of the Invention

The above mentioned problems associated with integrated circuit size and performance, the via and metal line formation process, and other problems are addressed by the present invention and will be understood by reading and studying the following specification. The structures and methods of the present invention include a diffusion barrier and a seed layer in an integrated circuit both formed using a low energy ion implantation followed by a selective deposition of metal lines for the integrated circuit. According to the teachings of the present invention, the selective deposition of the metal lines avoids the need for multiple chemical mechanical planarization (CMP) steps. The low energy ion implantation of the present invention allows for the distinct placement of both the diffusion barrier and the seed layer. A residual resist can be used to remove the diffusion barrier and the seed layer from unwanted areas on a wafer surface.

In particular one illustrative embodiment of the present invention includes a method of making a diffusion barrier and a seed layer in an integrated circuit. The method includes patterning an insulator material to define a number of trenches in the insulator layer opening to a number of first level vias in a planarized surface. A barrier/adhesion layer is deposited in the number of trenches using a low energy ion implantation, e.g. a 100 to 800 electron volt (eV) ion implantation. A seed layer is deposited on the barrier/adhesion layer in the number of trenches also using the low energy ion implantation. This novel methodology further accommodates the formation of aluminum, copper, gold, and/or silver metal interconnects.

Brief Description of the Drawings

The following detailed description of the preferred embodiments can best be understood when read in conjunction with the following drawings, in which:

Figure 1A-1K illustrate one embodiment of the various processing steps for forming vias and metal lines according to the teachings of the present invention;

Figure 2A-2K illustrate another embodiment of the various processing steps for forming vias and metal lines according to the teachings of the present invention;

Figure 3A-3K illustrate another embodiment of the various processing steps for forming vias and metal lines according to the teachings of the present invention;

Figure 4A-4L illustrate another embodiment of the various processing steps for forming vias and metal lines according to the teachings of the present invention;

Figure 5, is an illustration of an integrated circuit formed according to the teachings of the present invention.

Figure 6 illustrates an embodiment of a system including a portion of an integrated circuit formed according to any of the embodiments described in the present application.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Substrate include doped and unhoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term insulator is defined to include any material that is less electrically conductive than the materials generally referred to as conductors by those skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense.

What is disclosed herein is a low cost process to achieve reduced capacitance and resistance loss in wiring levels. The present invention requires

only one complete CMP planarizing coupled with the formation of the first level vias, no matter how many levels of metallurgy are used. What are essentially cleanup CMP steps on each metal level are used in one process sequence. This process can be used with an aluminum, copper, silver, gold or any other material which can subsequently be electrolessly plated or deposited by selective CVD or any other selective deposition process. A polyimide, other polymer or foam polymer can be used as an insulator. It can also be used with an oxide or other inorganic insulating structure if the insulating stack is compatible with the metal being used. It can also be used to form air bridge structures as well. The process uses low energy ion implantation to deposit both the adhesion and/or barrier layer along with the seed layer. This is coupled with using the resist layer which defines the damascene trench as the blocking layer to define the implant areas. Low energy implantation allows the placing of distinct layers of both barrier/adhesion and seed layers. The use of the same resist layers to define both the trench and seed layers allows a low cost implementation of the process.

Embodiment of a Metal Interconnect Using Copper and Polyimide

Figures 1A-1K illustrate a novel methodology for the formation of metal interconnects and/or a wiring structure in an integrated circuit according to the teachings of the present invention. The novel methodology includes the novel formation of a barrier/adhesion layer and a seed layer in an integrated circuit using a low energy ion implantation. The novel methodology also encompasses a novel method of making copper, silver, aluminum, or gold interconnect for an integrated circuit.

Figure 1A illustrates a portion of an integrated circuit structure, namely an integrated circuit having a number of semiconductor devices formed in a substrate. Figure 1 illustrates the structure after a device structure is formed in the substrate and the contact structure to the device structure is in place. One of ordinary skill in the art will understand upon reading this disclosure the manner in which a number of semiconductor structures, e.g. transistors, can be formed in a substrate. One of ordinary skill in the art will also understand upon reading this disclosure the manner in which a contact structure can be formed connecting to a given semiconductor device in a substrate. For example, Figure 1A illustrates the structure after a number of device structures, e.g. transistor 101A

photoresist 112 and then the first layer of polyimide 108 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that the first level metal pattern 110 is defined in the polyimide. According to the teachings of the present invention, a residual photoresist layer 112 is left in place on the first insulator layer 108 in a number of region 113 outside of the number trenches 110. The structure is now as appears in Figure 1B.

As shown in Figure 1C, a first barrier/adhesion layer 114 is deposited in the number of trenches 110 using a low energy ion implantation. In one embodiment according to the teachings of the present invention, depositing the barrier/adhesion layer 114 includes depositing a layer of zirconium 114 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the barrier/adhesion layer 114 includes depositing a barrier/adhesion layer 114 of titanium and/or hafnium. In one embodiment, depositing the depositing a layer of zirconium 114 includes depositing a layer of zirconium 114 having a thickness of approximately 50 Å. This can be achieved using a 10^{17} ion implant of zirconium, i.e. 10^{17} ions of zirconium per square centimeter (cm^2). According to the teachings of the present invention, the layer of zirconium 114 is implanted at 100 electron volts (eV) into the surface of the trenches 110 in the polymer layer 108 using a varying angle implant ($\propto$), as represented by arrows 111, where the angle of implantation is changed from normal to the wafer surface to 15 degrees off normal. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant, where an angle of implantation is changed from normal to the planarized surface 109 to approximately 15 degrees off normal deposits the barrier/adhesion layer 114 on all surfaces in the number of trenches 110. The structure is now as appears in Figure 1C.

In Figure 1D, a first seed layer 116 is deposited on the first barrier/adhesion layer 114 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the seed layer 116 on the barrier/adhesion layer 114 includes depositing a seed layer 116 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the seed layer 116 includes depositing a layer of copper 116 having a thickness of approximately a

100 Å. This can be achieved using an 8×10^{16} ion implant of copper. According to the teachings of the present invention, using a low energy ion implantation includes implanting the layer of copper 116 at 100 electron volts (eV) into the surface of the trenches 110 in the polymer layer. Also the layer of copper 116 is implanted at an angle normal to the wafer's surface, as shown by arrows 115. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 116 at an angle normal to the planarized surface results in the seed layer of copper 116 remaining on a bottom surface 118 in the number of trenches 110 and to a much lesser extent on the side surfaces 117 of the number of trenches 110. In one embodiment, an optional layer of aluminum 121 is deposited over the copper seed layer 116 again using a low energy ion implantation of 100 electron volts (eV). The optional layer of aluminum 121 is deposited to have a thickness of approximately a 50 Å. This can be achieved using a 3×10^{16} ion implant of aluminum normal to the wafer surface. As one of ordinary skill in the art will understand upon reading this disclosure, the layer of aluminum 121 is used to protect the copper seed layer 116 from oxidation prior to subsequent processing steps. The structure is now as shown in Figure 1D.

Figure 1E illustrates the structure after the next sequence of process steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 112 has served as a blocking layer to define the implant areas for the barrier/adhesion layer 114, the seed layer 116, and the layer of aluminum 121. The residual photoresist layer 112 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 112 includes removing the unwanted aluminum layer 121, the unwanted seed layer 116, and the unwanted barrier/adhesion layer 114 from other areas of the wafer's surface, e.g., from over a number of regions 113 outside of the trenches 110 on a top surface 119 of the first insulator layer 108. The structure is now as shown in Figure 1E.

In Figure 1F, a metallic conductor 120, or number of first level metal lines 120, is deposited over the seed layer 116 in the number of trenches 110. According to teachings of the present invention, metallic conductor 120, or

number of first level metal lines 120, is selected from the group consisting of aluminum, copper, silver, and gold depending on the type of seed layer 116 which was deposited. According to this embodiment, the metallic conductor 120, or number of first level metal lines 120 are selectively formed on the copper seed layer 116 such that the number of copper metal lines 120, or first level copper metal lines 120 are not formed on the top surface 119 of the first insulator layer 108. In one embodiment, the metallic conductor 120, or number of first level metal lines 120, is deposited using a selective CVD process. In another embodiment, depositing a metallic conductor 120, or number of first level metal lines 120, over the seed layer 116 includes depositing a metallic conductor 120 using electroless plating. Electroless copper plating is used to deposit sufficient copper to fill the number of trenches 110 to the top surface 119 of the first insulator layer 108.

As shown in Figure 1G, the process sequence may be continued to form any number of subsequent metal layers in a multilayer wiring structure. Figure 1G illustrates the structure after the next sequence of processing steps. In Figure 1G, a dual damascene process is used to define and fill a first to a second level of vias and a second level metallurgy. To do so, a second polymer layer 124, or second layer of polyimide 124, is deposited over the wafer surface, e.g. the metallic conductor 120, or number of first level metal lines 120, and the first polymer layer 108. The second polymer layer 124 may similarly be deposited using, for example, the process and material described in co-pending and commonly assigned application U. S. Serial No. 09/128,859, entitled "Copper Metallurgy in Integrated Circuits," which is hereby incorporated by reference. In one embodiment, depositing a second polymer layer 124 includes depositing a foamed second polymer layer 124. In one embodiment, the second polymer layer 124 is deposited and cured, forming a 10,000 Å thick second polymer layer 124 after curing. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the second polymer layer 124, or second insulator layer/material 124, may also be deposited as suited for forming a first to a second level of vias, e.g. second level vias, and a number of second level metal lines, the invention is not so limited. The second polymer layer 124, or second insulator layer/material 124 is patterned to define a second

level of vias and a number of second level metal lines in the second insulator layer/material 124 opening to the metallic conductor 120, or number of first level metal lines 120. In other words, a second level of vias is defined in a second mask layer of photoresist 126 and then the second polymer layer 124 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of via openings 128 are defined in the polyimide. Using the dual damascene process, a number of second level metal lines are also defined in a second mask layer of photoresist 126 and the second polymer layer 124 is again etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of metal line trenches 130 are defined in the polyimide. One of ordinary skill in the art will understand upon reading this disclosure, the manner in which a photoresist layer 126 can be mask, exposed, and developed using a dual damascene process to pattern a second level of via openings 128 and a second level of metal line trenches 130 in the second insulator layer/material 124.

As described previously, and according to the teachings of the present invention, a residual photoresist layer 126 is left in place on the second insulator layer/material 124 in a number of regions 132 outside of the second level of metal line trenches 130. A suitable plasma and/or wet cleaning process is used to remove any contaminates from the second level of via openings 128 and a second level of metal line trenches 130, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. The structure is now as appears in Figure 1G.

Figure 1H illustrates the structure 100 after the next sequence of processing steps. In Figure 1H, a second barrier/adhesion layer 134 is deposited in the second level of via openings 128 and a second level of metal line trenches 130 using a low energy ion implantation. As described above, in one embodiment according to the teachings of the present invention, depositing the second barrier/adhesion layer 134 includes depositing a layer of zirconium 134 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the second barrier/adhesion layer 134 includes depositing a barrier/adhesion layer 134 of titanium and/or hafnium. In one embodiment, depositing the layer of zirconium 134 includes depositing a layer of zirconium

134 having a thickness of approximately 50 Å. In one embodiment, this is achieved using a 10^{17} ion implant of zirconium. According to the teachings of the present invention, the layer of zirconium 134 is implanted at 100 electron volts (eV) into the surface of the second level of via openings 128 and a second level of metal line trenches 130 in the second polymer layer 124 using a varying angle, as shown by arrows 125, implant where the angle of implantation is changed from normal to the wafer surface to 15 degrees off normal. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant, where an angle of implantation is changed from normal to the wafer surface to approximately 15 degrees off normal deposits the barrier/adhesion layer 134 on all surfaces in the second level of via openings 128 and a second level of metal line trenches 130. The structure is now as appears in Figure 1H.

Figure 1I illustrates the structure 100 after the next sequence of processing steps. In Figure 1I, a second seed layer 136 is deposited on the second barrier/adhesion layer 134 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the second seed layer 136 on the second barrier/adhesion layer 114 includes depositing a second seed layer 136 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the second seed layer 136 includes depositing a second layer of copper 136 having a thickness of approximately a 100 Å. In one embodiment, this is achieved using an 8×10^{16} ion implant of copper. According to the teachings of the present invention, using a low energy ion implantation includes implanting the layer of copper 136 at 100 electron volts (eV) into the surfaces of the second level of via openings 128 and the polymer layer. Also the layer of copper 136 is implanted at an angle normal to the wafer's surface as shown by arrows 137. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 136 at an angle normal to the planarized surface results in the second seed layer of copper 136 remaining on a bottom surface 138 in the second level of via openings 128 and second level of metal line trenches 130 and to a much lesser extent on the side surfaces 140 of the second level of via openings 128 and a second level of metal line trenches

130. In one embodiment, an optional layer of aluminum 141 is deposited over the second copper seed layer 136 again using a low energy ion implantation of 100 electron volts (eV). The optional layer of aluminum is deposited to have a thickness of approximately a 50 Å. In one embodiment, this is achieved using a 3×10^{16} ion implant of aluminum normal to the wafer surface. As one of ordinary skill in the art will understand upon reading this disclosure, the layer of aluminum 141 is used to protect the second copper seed layer 136 from oxidation prior to subsequent processing steps.

FIG. 1J illustrates the structure after the next sequence of processing steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 126 has served as a blocking layer to define the implant areas for the second barrier/adhesion layer 134, the second seed layer 136, and the aluminum layer 141. The residual photoresist layer 126 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 126 includes removing the unwanted aluminum layer 141, the unwanted seed layer 136, and the unwanted barrier/adhesion layer 134 from other areas of the wafer's surface, e.g. from over a number of regions 132 outside of second level of metal line trenches 130 on a top surface 142 of the second insulator layer 124. The structure is now as shown in Figure 1J.

In Figure 1K, a second metallic conductor 144, or second core conductor 144, is deposited over or formed on the second seed layer 136 and within the second barrier/adhesion layer 134 in the second level of via openings 128 and the second level of metal line trenches 130 in the polymer layer. In this embodiment the second metallic conductor 144, or second core conductor 144, is copper, but in other embodiments of the present invention can be selected from the group consisting of aluminum, silver, and gold. In one embodiment, the second metallic conductor 144, or second core conductor 144, is deposited using a selective CVD process such that the second metallic conductor 144, or second core conductor 144 is not formed on a top surface 142 of the second insulator layer 124. In another embodiment, depositing a second metallic conductor 144, or second core conductor 144, over on the second seed layer 136 and within the

second barrier/adhesion layer 134 includes depositing a second metallic conductor 144, or second core conductor 144, using electroless plating. Electroless copper plating is used to deposit sufficient copper to fill the second level of via openings 128 and the second level of metal line trenches 130 to the top surface 142 of the second insulator layer 124. Thus, the second barrier/adhesion layer 134, the second seed layer 136, and the second metallic conductor 144, or second core conductor 144, constitute a second number of conductive structures which includes a number of second level vias and a number of second level metal lines which are formed over and connect to a first number of conductive structures, e.g. the first level metal lines 120.

Embodiment of a Metal Interconnect Using Aluminum Metal Lines and Oxide Insulators

Figures 2A-2K illustrate a novel methodology for the formation of metal interconnects and/or a wiring structure in an integrated circuit according to the teachings of the present invention. The novel methodology includes the novel formation of a barrier/adhesion layer and a seed layer in an integrated circuit using a low energy ion implantation. The novel methodology also encompasses a novel method of making copper, silver, aluminum, or gold interconnect for an integrated circuit.

Figure 2A illustrates a portion of an integrated circuit structure, namely an integrated circuit having a number of semiconductor devices formed in a substrate as described above in connection with Figure 1A. That is, Figure 2A illustrates the structure after a device structure is formed in the substrate and the contact structure to the device structure is in place. Like Figure 1A, Figure 2A illustrates the structure after a number of device structures, e.g. transistor 201A and 201B are formed in the substrate 200. An insulator layer 202 is deposited over the number of semiconductors 201A and 201B. The deposition of the insulator layer 202 can include depositing a layer of Si_3N_4 having a thickness in the range of 100 to 500 Angstroms (Å). This insulator layer will also serve as an additional barrier to impurities coming from subsequent processing steps. Contact holes 205A and 205B are opened to the number of device structures 201A and 201B using a photolithography technique. One of ordinary skill in the are will understand, upon reading this disclosure, the manner in which a

photolithography technique can be used to create contact holes 205A and 205B. In one embodiment of the present invention a titanium silicide liner 206A and 206B is placed in the contact holes 205A and 205B, such a through a process such as chemical vapor deposition (CVD). Next, tungsten vias 207A and 207B can be deposited in the contact holes 205A and 205B. The tungsten vias 207A and 207B can be deposited in the contact holes using any suitable technique such as using a CVD process. The excess tungsten is then removed from the wafer surface by chemical mechanical planarization (CMP) or other suitable processes to form a planarized surface 209.

As shown in Figure 2B, a first oxide layer 208, e.g. a silicon dioxide layer (SiO_2), is deposited over the wafer surface. In one embodiment, depositing a first oxide layer 208 includes depositing a fluorinated silicon oxide layer 208. The first oxide layer 208 may be deposited using any suitable technique, such as, for example, using a CVD process. In one embodiment, depositing a first oxide layer 208 having a thickness of approximately 5000 Å. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thicknesses for the first oxide layer 208 may also be deposited as suited for forming a first level metal pattern, the invention is not so limited. The first oxide layer 208 is patterned to define a number of trenches 210 in the first oxide layer 208 opening to a number of first level vias, e.g. tungsten vias 207A and 207B in planarized surface 209. In other words, a first level metal pattern 210 is defined in a mask layer of photoresist 212 and then the first oxide layer 208 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that the first level metal pattern 210 is defined in the first oxide layer 208. One of ordinary skill in the art will understand upon reading this disclosure that any desired first level metal pattern 210 can be created using a photolithography technique. According to the teachings of the present invention, a residual photoresist layer 212 is left in place on the first oxide layer 208 in a number of region 213 outside of the number trenches 210. The structure is now as appears in Figure 2B.

As shown in Figure 2C, a first barrier/adhesion layer 214 is deposited in the number of trenches 210 using a low energy ion implantation. In one embodiment according to the teachings of the present invention, depositing the barrier/adhesion layer 214 includes depositing a layer of zirconium 214 having a

thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the barrier/adhesion layer 214 includes depositing a barrier/adhesion layer 214 of titanium and/or hafnium. In one embodiment, depositing the depositing a layer of zirconium 214 includes depositing a layer of zirconium 214 having a thickness of approximately 50 Å. This can be achieved using a 10^{17} ion implant of zirconium. According to the teachings of the present invention, the layer of zirconium 214 is implanted at 100 electron volts (eV) into the surface of the trenches 210 in the first oxide layer 208 using a varying angle implant ($\propto$), as represented by arrows 211, where the angle of implantation is changed from normal to the wafer surface to 15 degrees off normal. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant, where an angle of implantation ($\propto$) is changed from normal to the wafer's surface to approximately 15 degrees off normal deposits the barrier/adhesion layer 214 on all surfaces in the number of trenches 210. The structure is now as appears in Figure 2C.

In Figure 2D, a first seed layer 216 is deposited on the first barrier/adhesion layer 214 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the seed layer 216 on the barrier/adhesion layer 214 includes depositing a first seed layer 216 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the seed layer 216 includes depositing a layer of an aluminum copper alloy 216 having a thickness of approximately 110 Å. This can be achieved by depositing a first layer of aluminum 281 on the barrier/adhesion layer 214 to a thickness of approximately 50 Å using a low energy ion implantation of approximately 100 electron volts (eV). A layer of copper 282 is then deposited on the first layer of aluminum 281 to a thickness of approximately 10 Å using a low energy ion implantation of approximately 100 eV. A second layer of aluminum 283 is then deposited on the layer of copper 282 to a thickness of approximately 50 Å using a low energy ion implantation of approximately 100 eV. Also the first seed layer 216 is implanted at an angle normal to the planarized surface, as shown by arrows 215. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the first seed layer 216 at an angle normal to the

planarized surface results in the first seed layer 216 remaining on a bottom surface 218 in the number of trenches 210 and to a much lesser extent on the side surfaces 217 of the number of trenches 210.

Figure 2E illustrates the structure after the next sequence of processing steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 212 has served as a blocking layer to define the implant areas for the barrier/adhesion layer 214 and the seed layer 216. The residual photoresist layer 212 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 212 includes removing the unwanted seed layer 216 and the unwanted barrier/adhesion layer 214 from other areas of the wafer's surface, e.g. from over a number of regions 213 outside of the trenches 210 on a top surface 219 of the first insulator layer 208. The structure is now as shown in Figure 2E.

In Figure 2F, a metallic conductor 220, or number of first level metal lines 220, is deposited over the first seed layer 216 and within the first barrier/adhesion layer 214 in the number of trenches 210. In this embodiment, the metallic conductor 220, or number of first level metal lines 220, is aluminum, but in other embodiments of the present invention the metallic conductor 220, or number of first level metal lines 220, is selected from the group consisting of copper, silver, and gold depending on the type of seed layer 216 which was deposited. In one embodiment, the metallic conductor 220, or number of first level metal lines 220, is deposited using a selective CVD process. In another embodiment, depositing a metallic conductor 220, or number of first level metal lines 220, over the seed layer 216 includes depositing a metallic conductor 220 using electroless plating. According to the teachings of the present invention the number of first level aluminum metal lines 220, is deposited to fill the number of trenches 210 to the top surface 219 of the first oxide layer 208. Thus, the first level aluminum metal lines 220, the first seed layer 216, and the first barrier/adhesion layer 214 in the number of trenches 210 constitute a first number of conductive structures. The copper composition of the first seed layer 216 can be adjusted to give the appropriate percentage of

copper in the completed first number of conductive structures. For example, in the above described embodiment the layer thicknesses of the aluminum copper sandwich was designed to give a 0.7 weight percent of copper in the first number of conductive structures.

As shown in Figure 2G, the process sequence may be continued to form any number of subsequent metal layers in a multilayer wiring structure. Figure 2G illustrates the structure after the next sequence of processing steps. In Figure 2G, a dual damascene process is used to define and fill a first to a second level of vias and a second level metallurgy. To do so, a second oxide layer 224 is deposited over the wafer surface, e.g. the metallic conductor 220, or number of first level metal lines 220, and the first oxide layer 208. In one embodiment, depositing a second oxide layer 224 includes depositing a second fluorinated silicon oxide layer 224. In one embodiment, the second oxide layer 224 is formed to have a thickness of approximately 10,000 Å. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the second oxide layer 224 may also be deposited as suited for forming a first to a second level of vias, e.g. second level vias, and a number of second level metal lines, the invention is not so limited. The second oxide layer 224 is patterned to define a second level of vias and a number of second level metal lines in the second oxide layer 224 opening to the metallic conductor 220, or number of first level metal lines 220. In other words, a second level of vias is defined in a second mask layer of photoresist 226 and then the second oxide layer 224 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of via openings 228 are defined in the polyimide. Using the dual damascene process, a number of second level metal lines are also defined in a second mask layer of photoresist 226 and the second oxide layer 224 is again etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of metal line trenches 230 are defined in the second oxide layer 224. One of ordinary skill in the art will understand upon reading this disclosure, the manner in which a photoresist layer 226 can be mask, exposed, and developed using a dual damascene process to pattern a second level of via openings 228 and a second level of metal line trenches 230 in the second oxide layer 224.

As described previously, and according to the teachings of the present invention, a residual photoresist layer 226 is left in place on the second oxide layer 224 in a number of regions 232 outside of the second level of metal line trenches 230. A suitable plasma and/or wet cleaning process is used to remove any contaminates from the second level of via openings 228 and a second level of metal line trenches 230, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. The structure is now as appears in Figure 2G.

Figure 2H illustrates the structure after the next sequence of processing steps. In Figure 2H, a second barrier/adhesion layer 234 is deposited in the second level of via openings 228 and a second level of metal line trenches 230 using a low energy ion implantation. As described above, in one embodiment according to the teachings of the present invention, depositing the second barrier/adhesion layer 234 includes depositing a layer of zirconium 234 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the second barrier/adhesion layer 234 includes depositing a barrier/adhesion layer 234 of titanium and/or hafnium. In one embodiment, depositing the layer of zirconium 234 includes depositing a layer of zirconium 234 having a thickness of approximately 50 Å. In one embodiment, this is achieved using a 10^{17} ion implant of zirconium (that is 10^{17} ions per square centimeter). According to the teachings of the present invention, the layer of zirconium 234 is implanted at 100 electron volts (eV) into the surface of the second level of via openings 228 and a second level of metal line trenches 230 in the second polymer layer 224 using a varying angle implant ($\propto$), as shown by arrows 225 where the angle of implantation is changed from normal to the wafer surface to 15 degrees off normal. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant, where an angle of implantation, $\propto$, is changed from normal to the wafer surface to approximately 15 degrees off normal deposits the barrier/adhesion layer 234 on all surfaces in the second level of via openings 228 and a second level of metal line trenches 230. The structure is now as appears in Figure 2H.

Figure 2I illustrates the structure after the next sequence of processing steps. In Figure 2I, a second seed layer 236 is deposited on the second

barrier/adhesion layer 234 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the second seed layer 236 on the second barrier/adhesion layer 214 includes depositing a second seed layer 236 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the seed layer 216 includes depositing a layer of an aluminum copper alloy 216 having a thickness of approximately 110 Å. This can be achieved by depositing a first layer of aluminum 284 on the barrier/adhesion layer 214 to a thickness of approximately 50 Å using a low energy ion implantation of approximately 100 electron volts (eV). A layer of copper 285 is then deposited on the first layer of aluminum 284 to a thickness of approximately 10 Å using a low energy ion implantation of approximately 100 eV. A second layer of aluminum 286 is then deposited on the layer of copper 285 to a thickness of approximately 50 Å using a low energy ion implantation of approximately 100 eV. Also the first seed layer 216 is implanted at an angle normal to the wafer's surface as shown by arrows 237. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 236 at an angle normal to the planarized surface results in the second seed layer of copper 236 remaining on a bottom surface 238 in the second level of via openings 228 and to a much lesser extent on the side surfaces 240 of the second level of via openings 228 and a second level of metal line trenches 230.

Figure 2J illustrates the structure following the next sequence of process steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 226 has served as a blocking layer to define the implant areas for the second barrier/adhesion layer 234 and the second seed layer 236. The residual photoresist layer 226 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 226 includes removing the unwanted barrier/adhesion layer 234 and the unwanted second seed layer 236, from other areas of the wafer's surface, e.g. from over a number of regions 232 outside of second level of metal line trenches 230 on a top surface 242 of the second oxide layer 224. The structure is now as shown in Figure 2J.

In Figure 2K, a second metallic conductor 244, or second core conductor 244, is deposited over or formed on the second seed layer 236 and within the second barrier/adhesion layer 234 in the second level of via openings 228 and the second level of metal line trenches 230 in the polymer layer. In this embodiment the second metallic conductor 244, or second core conductor 244, is aluminum, but in other embodiments of the present invention the second metallic conductor 244, or second core conductor 244, can be selected from the group consisting of copper, silver, and gold. In one embodiment, the second metallic conductor 244, or second core conductor 244, is deposited using a selective CVD process. In another embodiment, depositing a second metallic conductor 244, or second core conductor 244, over on the second seed layer 236 and within the second barrier/adhesion layer 234 includes depositing a second metallic conductor 244, or second core conductor 244, using electroless plating. The second aluminum conductor 244, or second core conductor 244 is deposited to fill the second level of via openings 228 and the second level of metal line trenches 230 to the top surface 242 of the second insulator layer 224. Thus, the second barrier/adhesion layer 234, the second seed layer 236, and the second metallic conductor 244, or second core conductor 244, constitute a second number of conductive structures which includes a number of second level vias and a number of second level metal lines which are formed over and connect to a first number of conductive structures, e.g. the first level of vias 207A and 207B.

Embodiment of a Metal Interconnect Using Copper Metal Lines and Oxide Insulators

Figures 3A-3K illustrate a novel methodology for the formation of metal interconnects and/or a wiring structure in an integrated circuit according to the teachings of the present invention. The novel methodology includes the novel formation of a barrier/adhesion layer and a seed layer in an integrated circuit using a low energy ion implantation. The novel methodology also encompasses a novel method of making copper, silver, aluminum, or gold interconnect for an integrated circuit.

Figure 3A illustrates a portion of an integrated circuit structure, namely an integrated circuit having a number of semiconductor devices formed in a substrate. Figure 3 illustrates the structure after a device structure is formed in

the substrate and the contact structure to the device structure is in place. One of ordinary skill in the art will understand upon reading this disclosure the manner in which a number of semiconductor structures, e.g. transistors, can be formed in a substrate. One of ordinary skill in the art will also understand upon reading this disclosure the manner in which a contact structure can be formed connecting to a given semiconductor device in a substrate, such as explained in connection with Figure 1A. For example, Figure 3A illustrates the structure after a number of device structures, e.g. transistor 301A and 301B are formed in the substrate 300. An insulator layer 302 is deposited over the number of semiconductors 301A and 301B. The deposition of the insulator layer 302 can include depositing a layer of Si_3N_4 having a thickness in the range of 100 to 500 Angstroms (Å). This insulator layer will also serve as an additional barrier to impurities coming from subsequent processing steps. Contact holes 305A and 305B are opened to the number of device structures 301A and 301B using a photolithography technique. One of ordinary skill in the are will understand, upon reading this disclosure, the manner in which a photolithography technique can be used to create contact holes 305A and 305B. In one embodiment of the present invention a titanium silicide liner 306A and 306B is placed in the contact holes 305A and 305B, such a through a process such as chemical vapor deposition (CVD). Next, tungsten vias 306A and 306B can be deposited in the contact holes 305A and 305B. The tungsten vias 307A and 307B can be deposited in the contact holes using any suitable technique such as using a CVD process. The excess tungsten is then removed from the wafer surface by chemical mechanical planarization (CMP) or other suitable processes to form a planarized surface 309.

As shown in Figure 3B, a first polymer layer 308, or first layer of polyimide 308, is deposited over the wafer surface. The first oxide layer 308 may be deposited using any suitable technique such as, for example, a CVD process. In one embodiment, depositing a first oxide layer 308 includes depositing a fluorinated silicon oxide layer 308. In one embodiment, the first oxide layer 308 is deposited to have a thickness of approximately 5000 Å. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the first oxide layer 308 may also be deposited as

suited for forming a first level metal pattern, the invention is not so limited. The first oxide layer 308 is patterned to define a number of trenches 310 in the first oxide layer 308 opening to a number of first level vias, e.g. tungsten vias 307A and 307B in planarized surface 309. In other words, a first level metal pattern 310 is defined in a mask layer of photoresist 312 and then the first oxide layer 308 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that the first level metal pattern 310 is defined in the first oxide layer 308. According to the teachings of the present invention, a residual photoresist layer 312 is left in place on the first oxide layer 308 in a number of region 313 outside of the number trenches 310. The structure is now as appears in Figure 3B.

As shown in Figure 3C, a first barrier/adhesion layer 314 is deposited in the number of trenches 310 using a low energy ion implantation. In one embodiment according to the teachings of the present invention, depositing the barrier/adhesion layer 314 includes depositing a tantalum nitride layer 314 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the barrier/adhesion layer 314 includes depositing a barrier/adhesion layer 314 of tantalum and/or CuTi. In one embodiment, depositing the tantalum nitride layer 314 includes first depositing a layer of tantalum 381 to have a thickness of approximately 100 Å using a low energy ion implantation of approximately 100 electron volts (eV) at a varying angle implant ($\propto$), e.g. the angle of implantation ($\propto$) is changed from normal to the planarized surface 309 to approximately 15 degrees off normal as shown by arrows 311. In one embodiment, this is achieved using a 10^{17} ion implant of tantalum. Next, according to the teachings of the present invention, a layer of nitrogen 382 is implanted at 700 electron volts (eV) into the layer of tantalum 381. In one embodiment, this is achieved using an 8×10^{16} ion implant of nitrogen. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant, where an angle of implantation is changed from normal to the planarized surface 309 to approximately 15 degrees off normal deposits the barrier/adhesion layer 314 on all surfaces in the number of trenches 310. The structure is now as appears in Figure 3C.

In Figure 3D, a first seed layer 316 is deposited on the first barrier/adhesion layer 314 using a low energy ion implantation. According to

the broader teachings of the present invention, depositing the seed layer 316 on the barrier/adhesion layer 314 includes depositing a seed layer 316 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the seed layer 316 includes depositing a layer of copper 316 having a thickness of approximately 50 Å. This can be achieved using an 8×10^{16} ion implant of copper. According to the teachings of the present invention, using a low energy ion implantation includes implanting the layer of copper 316 at 100 electron volts (eV) into the first barrier/adhesion layer 314. Also the layer of copper 316 is implanted at an angle normal to the planarized surface 309 as shown by arrows 315. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 316 at an angle normal to the planarized surface results in the seed layer of copper 316 remaining on a bottom surface 318 in the number of trenches 310 and to a much lesser extent on the side surfaces 320 of the number of trenches 310. In one embodiment, an optional layer of aluminum 321 is deposited over the copper seed layer 316 again using a low energy ion implantation of 100 electron volts (eV). The optional layer of aluminum 321 is deposited to have a thickness of approximately a 50 Å. This can be achieved using a 3×10^{16} ion implant of aluminum normal to the wafer surface. As one of ordinary skill in the art will understand upon reading this disclosure, the layer of aluminum 321 is used to protect the copper seed layer 316 from oxidation prior to subsequent processing steps. The structure is now as appears in Figure 3D.

Figure 3E illustrates the structure after the next sequence of processing steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 312 has served as a blocking layer to define the implant areas for the barrier/adhesion layer 314, the seed layer 316, and the layer of aluminum 321. The residual photoresist layer 312 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 312 includes removing the unwanted aluminum layer 321, the unwanted seed layer 316, and the unwanted barrier/adhesion layer 314 from other areas of the wafer's surface,

e.g. from over a number of regions outside of the trenches 310 on a top surface 319 of the first insulator layer 308. The structure is now as shown in Figure 3E.

In Figure 3F, a metallic conductor 320, or number of first level metal lines 320, is deposited over the seed layer 316 in the number of trenches 310. According to teachings of the present embodiment, the metallic conductor 320, or number of first level metal lines 320, is copper. In one embodiment, the metallic conductor 320, or number of first level metal lines 320, is deposited using a selective CVD process. In another embodiment, depositing a metallic conductor 320, or number of first level metal lines 320, over the seed layer 316 includes depositing a metallic conductor 320 using electroless plating. Electroless copper plating is used to deposit sufficient copper to fill the number of trenches 310 to a level approximately 100 Å below the top surface 319 of the first oxide layer 308. At this point, a second layer of tantalum nitride 323 is deposited to a thickness of approximately 100 Å on the copper metallic conductor 320, or number of first level copper lines 320. A chemical mechanical planarization (CMP) cleanup process is then used to remove the tantalum nitride from the top surface 319 of the first oxide layer 308.

As shown in Figure 3G, the process sequence may be continued to form any number of subsequent metal layers in a multilayer wiring structure. Figure 3G illustrates the structure after the next sequence of processing steps. In Figure 3G, a dual damascene process is used to define and fill a first to a second level of vias and a second level metallurgy. To do so, a second oxide layer 324 is deposited over the wafer surface, e.g. the metallic conductor 320, or number of first level metal lines 320, and the first oxide layer 308. The second oxide layer 324 is again deposited using any suitable technique. In one embodiment, depositing a second oxide layer 324 includes depositing a fluorinated silicon oxide layer 324. In one embodiment, the second oxide layer 324 is deposited to have a thickness of approximately 10,000 Å. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the second oxide layer 324 may also be deposited as suited for forming a first to a second level of vias, e.g. second level vias, and a number of second level metal lines, the invention is not so limited. The second oxide layer 324 is patterned to define a second level of vias and a number of second level metal lines in the

second oxide layer 324 opening to the metallic conductor 320, or number of first level metal lines 320. In other words, a second level of vias is defined in a second mask layer of photoresist 326 and then the second oxide layer 324 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of via openings 328 are defined in the second oxide layer 324. Using the dual damascene process, a number of second level metal lines are also defined in a second mask layer of photoresist 326 and the second oxide layer 324 is again etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of metal line trenches 330 are defined in the oxide. One of ordinary skill in the art will understand upon reading this disclosure, the manner in which a photoresist layer 326 can be mask, exposed, and developed using a dual damascene process to pattern a second level of via openings 328 and a second level of metal line trenches 330 in the second oxide layer 324.

As described previously, and according to the teachings of the present invention, a residual photoresist layer 326 is left in place on the second oxide layer 324 in a number of regions 332 outside of the second level of metal line trenches 330. A suitable plasma and/or wet cleaning process is used to remove any contaminates from the second level of via openings 328 and a second level of metal line trenches 330, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. The structure is now as appears in Figure 3G.

Figure 3H illustrates the structure after the next sequence of processing steps. In Figure 3H, a second barrier/adhesion layer 334 is deposited in the second level of via openings 328 and a second level of metal line trenches 330 using a low energy ion implantation. As described above, in one embodiment according to the teachings of the present invention, depositing the second barrier/adhesion layer 334 includes depositing a tantalum nitride layer 334 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the second barrier/adhesion layer 334 includes depositing a second barrier/adhesion layer 334 of tantalum and/or CuTi. In one embodiment, depositing the tantalum nitride layer 334 includes first depositing a layer of tantalum 383 to have a thickness of approximately 100 Å using a low energy ion implantation of approximately 100 electron volts (eV) at a varying angle implant

(∝), e.g. the angle of implantation (∝) is changed from normal to the wafer's surface to approximately 15 degrees off normal as shown by arrows 325. In one embodiment, this is achieved using a 10^{17} ion implant of tantalum. Next, according to the teachings of the present invention, a layer of nitrogen 384 is implanted at 700 electron volts (eV) into the layer of tantalum 383. In one embodiment, this is achieved using an 8×10^{16} ion implant of nitrogen. As one of ordinary skill in the art will understand upon reading this disclosure, using a varying angle implant (∝), where an angle of implantation is changed from normal to the wafer's surface to approximately 15 degrees off normal deposits the second barrier/adhesion layer 334 on all surfaces in the second level of via openings 328 and in the second level of metal line trenches 330 formed in the second oxide layer 324. The structure is now as appears in Figure 3H.

Figure 3I illustrates the structure after the next sequence of processing steps. In Figure 3I, a second seed layer 336 is deposited on the second barrier/adhesion layer 334 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the second seed layer 336 on the second barrier/adhesion layer 314 includes depositing a second seed layer 336 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the second seed layer 336 includes depositing a second layer of copper 336 having a thickness of approximately 50 Å. In one embodiment, this is achieved using an 8×10^{16} ion implant of copper. According to the teachings of the present invention, using a low energy ion implantation includes implanting the layer of copper 336 at 100 electron volts (eV) into the surfaces of the second level of via openings 328 and the second level of metal line trenches 330 in the polymer layer. Also the layer of copper 336 is implanted at an angle normal to the wafer's surface as shown by arrows 337. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 336 at an angle normal to the wafer's surface results in the second seed layer of copper 336 remaining on a bottom surface 338 in the second level of via openings 328 and to a much lesser extent on the side surfaces 340 of the second level of via openings 328 and a second level of metal line trenches 330. In one embodiment, an optional layer of aluminum 341 is deposited over the second

copper seed layer 336 again using a low energy ion implantation of 100 electron volts (eV). The optional layer of aluminum is deposited to have a thickness of approximately a 50 Å. In one embodiment, this is achieved using a 3×10^{16} ion implant of aluminum normal to the wafer surface. As one of ordinary skill in the art will understand upon reading this disclosure, the layer of aluminum 341 is used to protect the second copper seed layer 336 from oxidation prior to subsequent processing steps. The structure is now as shown in Figure 3I.

Figure 3J illustrates the structure after the next sequence of processing steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 326 has served as a blocking layer to define the implant areas for the second barrier/adhesion layer 334, the second seed layer 336, and the aluminum layer 341. The residual photoresist layer 326 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 326 includes removing the unwanted aluminum layer 341, the unwanted seed layer 336, and the unwanted barrier/adhesion layer 334 from other areas of the wafer's surface, e.g. from over a number of regions 332 outside of second level of metal line trenches 330 on a top surface 342 of the second insulator layer 324. The structure is now as shown in Figure 3J.

In Figure 3K, a second metallic conductor 344, or second core conductor 344, is deposited over or formed on the second seed layer 336 and within the second barrier/adhesion layer 334 in the second level of via openings 328 and the second level of metal line trenches 330 in the polymer layer. In this embodiment the second metallic conductor 344, or second core conductor 344, is copper, but in other embodiments of the present invention the second metallic conductor 344, or second core conductor 344, can be selected from the group consisting of aluminum, silver, and gold. In one embodiment, the second metallic conductor 344, or second core conductor 344, is deposited using a selective CVD process. In another embodiment, depositing a second metallic conductor 344, or second core conductor 344, over on the second seed layer 336 and within the second barrier/adhesion layer 334 includes depositing a second metallic conductor 344, or second core conductor 344, using electroless plating. Electroless copper

plating is used to deposit sufficient copper to fill the second level of via openings 328 and the second level of metal line trenches 330 to level approximately 100 Å below the top surface 342 of the second insulator layer 324. At this point, a second layer of tantalum nitride 346 is deposited to a thickness of approximately 100 Å on the second metallic conductor 344, or second core conductor 344. A chemical mechanical planarization (CMP) cleanup process is then used to remove the tantalum nitride from the top surface 342 of the second insulator layer 324. Thus, the second barrier/adhesion layer 334, the second seed layer 336, and the second metallic conductor 344, or second core conductor 344, constitute a second number of conductive structures which includes a number of second level vias and a number of second level metal lines which are formed over and connect to a first number of conductive structures, e.g. the metallic conductor 320, or number of first level metal lines 320.

Another Embodiment of a Metal Interconnect Using Copper

Figures 4A-4L illustrate a novel methodology for the formation of metal interconnects and/or a wiring structure in an integrated circuit according to the teachings of the present invention. The novel methodology includes the novel formation of a barrier/adhesion layer and a seed layer in an integrated circuit using a low energy ion implantation. The novel methodology also encompasses a novel method of making copper, silver, aluminum, or gold interconnect for an integrated circuit.

Figure 4A illustrates a portion of an integrated circuit structure, namely an integrated circuit having a number of semiconductor devices formed in a substrate. Figure 4A illustrates the structure after a device structure is formed in the substrate and the contact structure to the device structure is in place. One of ordinary skill in the art will understand upon reading this disclosure the manner in which a number of semiconductor structures, e.g. transistors, can be formed in a substrate. One of ordinary skill in the art will also understand upon reading this disclosure the manner in which a contact structure can be formed connecting to a given semiconductor device in a substrate, such as described in connection with Figure 1A. For example, Figure 4A illustrates the structure after a number of device structures, e.g. transistor 401A and 401B are formed in the substrate 400. An insulator layer 402 is deposited over the number of semiconductors

401A and 401B. The deposition of the insulator layer 402 can include depositing a layer of Si_3N_4 having a thickness in the range of 100 to 500 Angstroms (Å). This insulator layer will also serve as an additional barrier to impurities coming from subsequent processing steps. Contact holes 405A and 405B are opened to the number of device structures 401A and 401B using a photolithography technique. One of ordinary skill in the are will understand, upon reading this disclosure, the manner in which a photolithography technique can be used to create contact holes 405A and 405B. In one embodiment of the present invention a titanium silicide liner 406A and 406B is placed in the contact holes 405A and 405B, such a through a process such as chemical vapor deposition (CVD). Next, tungsten vias 407A and 407B can be deposited in the contact holes 405A and 405B. The tungsten vias 407A and 407B can be deposited in the contact holes using any suitable technique such as using a CVD process. The excess tungsten is then removed from the wafer surface by chemical mechanical planarization (CMP) or other suitable processes to form a planarized surface 409.

As shown in Figure 4B, a first polymer layer 408, or first layer of polyimide 408, is deposited over the wafer surface. The first polymer layer 408 may be deposited using, for example, the process and material described in co-pending and commonly assigned application U. S. Serial No. 09/128,859, entitled "Copper Metallurgy in Integrated Circuits," which is hereby incorporated by reference. In one embodiment, depositing a first polymer layer 408 includes depositing a foamed polymer layer 408. In one embodiment, the first layer of polyimide 408 is deposited and cured, forming a 5000 Å thick layer of polymer 408 after curing. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the first layer of polyimide 408, or insulator layer/material 408, may also be deposited as suited for forming a first level metal pattern, the invention is not so limited. The first layer of polyimide 408, or first insulator layer/material 408 is patterned to define a number of trenches 410 in the first insulator layer 408 opening to a number of first level vias, e.g. tungsten vias 407A and 407B in planarized surface 409. In other words, a first level metal pattern 410 is defined in a mask layer of photoresist 412 and then the first layer of polyimide 408 is etched, using any

suitable process, e.g. reactive ion etching (RIE), such that the first level metal pattern 410 is defined in the polyimide. According to the teachings of the present invention, a residual photoresist layer 412 is left in place on the first insulator layer 408 in a number of region 413 outside of the number trenches 410. The structure is now as appears in Figure 4B.

As shown in Figure 4C, a first barrier/adhesion layer 414 is deposited in the number of trenches 410 using a low energy ion implantation. In one embodiment according to the teachings of the present invention, depositing the barrier/adhesion layer 414 includes depositing a layer of zirconium 414 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the barrier/adhesion layer 414 includes depositing a barrier/adhesion layer 414 of titanium and/or hafnium. In one embodiment, depositing the depositing a layer of zirconium 414 includes depositing a layer of zirconium 414 having a thickness of approximately 15 Å. This can be achieved using a 10^{17} ion implant of zirconium. According to the teachings of the present invention, the layer of zirconium 414 is implanted at 100 electron volts (eV) into the surface of the trenches 410 in the polymer layer 408 using an angle of implant normal to the wafer's surface as shown by arrows 411. The structure is now as appears in Figure 4C.

In Figure 4D, a first seed layer 416 is deposited on the first barrier/adhesion layer 414 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the seed layer 416 on the barrier/adhesion layer 414 includes depositing a seed layer 416 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the seed layer 416 includes depositing a layer of copper 416 having a thickness of approximately a 50 Å. This can be achieved using an 8×10^{16} ion implant of copper. According to the teachings of the present invention, using a low energy ion implantation includes implanting the layer of copper 416 at 100 electron volts (eV) into the surface of the trenches 410 in the polymer layer. Also the layer of copper 416 is implanted at an angle normal to the wafer's surface as shown by arrows 415. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 416 at an angle normal to the wafer's surface

results in the seed layer of copper 416 remaining on a bottom surface 418 in the number of trenches 410 and to a much lesser extent on the side surfaces 420 of the number of trenches 410. In one embodiment, an optional layer of aluminum 421 is deposited over the copper seed layer 416 again using a low energy ion implantation of 100 electron volts (eV). The optional layer of aluminum 421 is deposited to have a thickness of approximately a 50 Å. This can be achieved using a 3×10^{16} ion implant of aluminum normal to the wafer surface as shown by arrows 415. As one of ordinary skill in the art will understand upon reading this disclosure, the layer of aluminum 421 is used to protect the copper seed layer 416 from oxidation prior to subsequent processing steps. The structure is now as appears in Figure 4D.

Figure 4E illustrates the structure after the next sequence of processing steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 412 has served as a blocking layer to define the implant areas for the barrier/adhesion layer 414, the seed layer 416, and the layer of aluminum 421. The residual photoresist layer 412 is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 412 includes removing the unwanted aluminum layer 421, the unwanted seed layer 416, and the unwanted barrier/adhesion layer 414 from other areas of the wafer's surface, e.g. from over a number of regions 413 outside of the trenches 410 on a top surface 419 of the first insulator layer 408. The structure is now as shown in Figure 4E.

In Figure 4F, a metallic conductor 420, or number of first level metal lines 420, is deposited over the seed layer 416 in the number of trenches 410. According to teachings of the metallic conductor 420, or number of first level metal lines 420, is selected from the group consisting of aluminum, copper, silver, and gold depending on the type of seed layer 416 which was deposited. According to this embodiment, a number of copper metal lines 420, or first level copper metal lines 420 are selectively formed on the copper seed layer 416. In one embodiment, the metallic conductor 420, or number of first level metal lines 420, is deposited using a selective CVD process. In another embodiment,

23. A method of making a diffusion barrier and a seed layer in an integrated circuit assembly, comprising:

depositing an oxide layer having a thickness suitable for a first level metal interconnect over a planarized surface;

etching the oxide layer using a mask layer of photoresist to define a number of trenches in the oxide layer opening to a number of first level vias in the planarized surface;

depositing a layer of tantalum in the number of trenches, wherein the layer of tantalum has a thickness of approximately 100 Angstroms and is deposited using a low energy ion implantation of approximately 100 electron volts;

depositing a layer of Nitrogen on the layer of tantalum using a low energy ion implantation of approximately 700 electron volts;

depositing a seed layer of Copper on layer of Nitrogen in the number of trenches having a thickness of approximately 100 Angstroms using a low energy ion implantation of approximately 100 electron volts; and

depositing a metallic conductor over the seed layer using a selective deposition process.

24. The method of claim 23, wherein depositing a layer of tantalum using a low energy ion implantation of approximately 100 electron volts includes varying an angle of implantation wherein the angle is varied from an angle normal to the planarized surface to an angle 15 degrees off normal.

25. The method of claim 23, wherein depositing a layer of Nitrogen on the layer of tantalum using a low energy ion implantation of approximately 700 electron volts includes varying an angle of implantation wherein the angle is varied from an angle normal to the planarized surface to an angle 15 degrees off normal.

26. The method of claim 23, wherein depositing a seed layer of Copper on the barrier/adhesion layer in the number of trenches using a low energy ion

depositing a metallic conductor 420, or number of first level metal lines 420, over the seed layer 416 includes depositing a metallic conductor 420 using electroless plating. Electroless copper plating is used to deposit sufficient copper to fill the number of trenches 410 to the top surface 419 of the first insulator layer 408.

As shown in Figure 4G, the process sequence may be continued to form any number of subsequent metal layers in a multilayer wiring structure. Figure 4G illustrates the structure after the next sequence of processing steps. In Figure 4G, a dual damascene process is used to define and fill a first to a second level of vias and a second level metallurgy. To do so, a second polymer layer 424, or second layer of polyimide 424, is deposited over the wafer surface, e.g. the metallic conductor 420, or number of first level metal lines 420, and the first polymer layer 408. The second polymer layer 424 may similarly be deposited using, for example, the process and material described in co-pending and commonly assigned application U. S. Serial No. 09/128,859, entitled "Copper Metallurgy in Integrated Circuits," which is hereby incorporated by reference. In one embodiment, depositing a second polymer layer 424 includes depositing a foamed second polymer layer 424. In one embodiment, the second polymer layer 424 is deposited and cured, forming a 10,000 Å thick second polymer layer 424 after curing. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the second polymer layer 424, or second insulator layer/material 424, may also be deposited as suited for forming a first to a second level of vias, e.g. second level vias, and a number of second level metal lines, the invention is not so limited. The second polymer layer 424, or second insulator layer/material 424 is patterned to define a second level of vias and a number of second level metal lines in the second insulator layer/material 424 opening to the metallic conductor 420, or number of first level metal lines 420. In other words, a second level of vias is defined in a second mask layer of photoresist 426 and then the second polymer layer 424 is etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of via openings 428 are defined in the polyimide. Using the dual damascene process, a number of second level metal lines are also defined in a second mask layer of photoresist 426 and the second polymer layer 424 is again

etched, using any suitable process, e.g. reactive ion etching (RIE), such that a second level of metal line trenches 430 are defined in the polyimide. One of ordinary skill in the art will understand upon reading this disclosure, the manner in which a photoresist layer 426 can be mask, exposed, and developed using a dual damascene process to pattern a second level of via openings 428 and a second level of metal line trenches 430 in the second insulator layer/material 424.

As described previously, and according to the teachings of the present invention, a residual photoresist layer 426 is left in place on the second insulator layer/material 424 in a number of regions 432 outside of the second level of metal line trenches 430. A suitable plasma and/or wet cleaning process is used to remove any contaminates from the second level of via openings 428 and a second level of metal line trenches 430, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. The structure is now as appears in Figure 4G.

Figure 4H illustrates the structure after the next sequence of processing steps. In Figure 4H, a second barrier/adhesion layer 434 is deposited in the second level of via openings 428 and a second level of metal line trenches 430 using a low energy ion implantation. As described above, in one embodiment according to the teachings of the present invention, depositing the second barrier/adhesion layer 434 includes depositing a layer of zirconium 434 having a thickness of approximately 5 to 100 Å. In alternate embodiments, depositing the second barrier/adhesion layer 434 includes depositing a barrier/adhesion layer 434 of titanium and/or hafnium. In one embodiment, depositing the layer of zirconium 434 includes depositing a layer of zirconium 434 having a thickness of approximately 15 Å. In one embodiment, this is achieved using a 10^{17} ion implant of zirconium. According to the teachings of the present invention, the layer of zirconium 434 is implanted at 100 electron volts (eV) into the surface of the second level of via openings 428 and a second level of metal line trenches 430 in the second polymer layer 424 using an implant angle normal to the wafer's surface as shown by arrows 425. The structure is now as appears in Figure 4H.

Figure 4I illustrates the structure after the next sequence of processing steps. In Figure 4I, a second seed layer 436 is deposited on the second barrier/adhesion layer 434 using a low energy ion implantation. According to the broader teachings of the present invention, depositing the second seed layer 436 on the second barrier/adhesion layer 414 includes depositing a second seed layer 436 selected from the group consisting of aluminum, copper, silver, and gold. However, according to the teachings of the present embodiment, depositing the second seed layer 436 includes depositing a second layer of copper 436 having a thickness of approximately a 50 Å. In one embodiment, this is achieved using an 8×10^{16} ion implant of copper. According to the teachings of the present invention, using a low energy ion implantation includes implanting the layer of copper 436 at 100 electron volts (eV) into the second level of via openings 428 and the second level of metal line trenches 430 in the polymer layer. Also the layer of copper 436 is implanted at an angle normal to the wafer's surface as shown by arrows 437. As one of ordinary skill in the art will understand upon reading this disclosure, implanting the layer of copper 436 at an angle normal to the wafer's surface results in the second seed layer of copper 436 remaining on a bottom surface 438 in the second level of via openings 428 and to a much lesser extent on the side surfaces 440 of the second level of via openings 428 and a second level of metal line trenches 430. In one embodiment, an optional layer of aluminum 441 is deposited over the second copper seed layer 436 again using a low energy ion implantation of 100 electron volts (eV). The optional layer of aluminum is deposited to have a thickness of approximately a 50 Å. In one embodiment, this is achieved using a 3×10^{16} ion implant of aluminum normal to the wafer surface. As one of ordinary skill in the art will understand upon reading this disclosure, the layer of aluminum 441 is used to protect the second copper seed layer 436 from oxidation prior to subsequent processing steps. The structure is now as appears in Figure 4I.

Figure 4J illustrates the structure after the next sequence of processing steps. As one of ordinary skill in the art will understand upon reading this disclosure, the residual photoresist layer 426 has served as a blocking layer to define the implant areas for the second barrier/adhesion layer 434, the second seed layer 436, and the aluminum layer 441. The residual photoresist layer 426

is now removed using a wet strip process, as the same will be understood by one of ordinary skill in the art upon reading this disclosure. According to the teachings of the present invention, removing the residual photoresist layer 426 includes removing the unwanted aluminum layer 441, the unwanted seed layer 436, and the unwanted barrier/adhesion layer 434 from other areas of the wafer's surface, e.g. from over a number of regions 432 outside of second level of metal line trenches 430 on a top surface 442 of the second insulator layer 424. The structure is now as shown in Figure 4J.

In Figure 4K, a second metallic conductor 444, or second core conductor 444, is deposited over or formed on the second seed layer 436 and within the second barrier/adhesion layer 434 in the second level of via openings 428 and the second level of metal line trenches 430 in the polymer layer. In this embodiment the second metallic conductor 444, or second core conductor 444, is copper, but in other embodiments of the present invention the second metallic conductor 444, or second core conductor 444, can be selected from the group consisting of aluminum, silver, and gold. In one embodiment, the second metallic conductor 444, or second core conductor 444, is deposited using a selective CVD process. In another embodiment, depositing a second metallic conductor 444, or second core conductor 444, over on the second seed layer 436 and within the second barrier/adhesion layer 434 includes depositing a second metallic conductor 444, or second core conductor 444, using electroless plating. Electroless copper plating is used to deposit sufficient copper to fill the second level of via openings 428 and the second level of metal line trenches 430 to the top surface 442 of the second insulator layer 424. Thus, the second barrier/adhesion layer 434, the second seed layer 436, and the second metallic conductor 444, or second core conductor 444, constitute a second number of conductive structures which includes a number of second level vias and a number of second level metal lines which are formed over and connect to a first number of conductive structures, e.g. the metallic conductor 420, or number of first level metal lines 420.

As one of ordinary skill in the art will understand upon reading this disclosure, the above described method embodiments can be repeated until the requisite number of metal layers are formed.

Figure 4L illustrates the structure following the final sequence of processing steps. Upon completion of the last level of metal, the entire polymer structure, e.g. first polymer layer 408 and second polymer layer 424, are removed using an O_2 plasma etch. The structure is now as appears in Figure 4L.

Figure 5, is an illustration of an embodiment of an integrated circuit formed according to the teachings of the present invention. As shown in Figure 5, the integrated circuit includes a metal layer in an integrated circuit. The metal layer includes a number of first level vias 507A and 507B connecting to a number of silicon devices 501A and 501B in a substrate 500. A number of first level metal lines 520 are formed above and connect to the number of first level vias 507A and 507B. A barrier/adhesion layer 518 having a thickness in the range of 5 to 150 Angstroms is formed on the number of first level metal lines 520. A seed layer 516 having a thickness in the range of 5 to 150 Angstroms is formed at least between a portion of the barrier/adhesion layer 518 and the number of first level metal lines 520. As described above the barrier adhesion layer 50 having a thickness in the range of 5 to 150 Angstroms includes a barrier/adhesion layer selected from the group consisting of titanium, zirconium, and hafnium. In one embodiment, as shown in Figure 5, the number of first level vias 507A and 507B connecting to a number of silicon devices 501A and 501B in substrate 500 are surrounded by an insulator layer.

As described above the number of first level metal lines 502 includes a number of first level metal lines 520 is selected from the group consisting of Aluminum, Copper, Silver, and Gold. In one embodiment, the integrated circuit 503 comprises a portion of an integrated memory circuit 503. In this embodiment, the number of silicon devices 501A and 501B includes one or more transistors 501A and 501B in the substrate 500.

As one of ordinary skill in the art will understand upon reading this disclosure, any one of the embodiments as shown in Figures 1K, 2K, 3K, and/or 4L can comprise a portion of an integrated circuit according to the teachings of the present invention.

Figure 6 illustrates an embodiment of a system 600 including a portion of an integrated circuit formed according to any of the embodiments described in the present application. As one of ordinary skill in the art will understand upon

reading this disclosure, this system 600 includes a processor 610 and an integrated circuit, or integrated memory circuit 630 coupled to the processor 610. The processor 610 can be coupled to the integrated memory circuit 630 via any suitable bus, as the same are known and understood by one of ordinary skill in the art. In the embodiment, the processor 610 and integrated circuit 630 are located on a single wafer or die. Again, at least a portion of the integrated circuit 630 includes a portion of an integrated circuit 603 as disclosed in the various embodiments provided herein.

Conclusion

Thus, structures and methods have been provided which improve the performance of integrated circuits according to shrinking design rules. The structures and methods include a diffusion barrier and a seed layer in an integrated circuit both formed using a low energy ion implantation followed by a selective deposition of metal lines for the integrated circuit. According to the teachings of the present invention, the selective deposition of the metal lines avoids the need for multiple chemical mechanical planarization (CMP) steps. The low energy ion implantation of the present invention allows for the distinct placement of both the diffusion barrier and the seed layer. A residual resist can be used to remove the diffusion barrier and the seed layer from unwanted areas on a wafer surface. The structures formed by the described novel processes accommodate aluminum, copper, gold, and silver metal interconnects.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed:

1. A method of making a diffusion barrier and a seed layer in an integrated circuit assembly, comprising:

patterning an insulator material to define a number of trenches in the insulator layer opening to a number of first level vias in a planarized surface;

depositing a barrier/adhesion layer in the number of trenches using a low energy ion implantation; and

depositing a seed layer on the barrier/adhesion layer in the number of trenches using a low energy ion implantation.

2. The method of claim 1, wherein using a low energy ion implantation includes using a 100 to 800 electron volt (eV) ion implantation.

3. The method of claim 1, wherein patterning an insulator material includes patterning a polyimide.

4. The method of claim 1, wherein depositing a barrier/adhesion layer includes depositing a barrier/adhesion layer selected from the group consisting of Titanium, Zirconium, and Hafnium.

5. The method of claim 4, wherein depositing a barrier/adhesion layer includes depositing a barrier/adhesion layer having a thickness in the range of 5 to 100 Angstroms.

6. The method of claim 1, wherein the method further includes depositing a metallic conductor over the seed layer in the number of trenches, wherein the metallic conductor is selected from the group consisting of Aluminum, Copper, Silver, and Gold.

7. The method of claim 6, wherein depositing a metallic conductor over the seed layer includes depositing a metallic conductor using electroless plating.

8. The method of claim 1, wherein depositing a seed layer on the barrier/adhesion layer includes depositing a seed layer selected from the group consisting of Aluminum, Copper, Silver, and Gold.

9. A method of making copper, silver, or gold interconnect for an integrated circuit, comprising:

depositing an insulator layer having a thickness suitable for a first level metal interconnect over a planarized surface;

etching the insulator layer using a mask layer of photoresist to define a number of trenches in the insulator layer opening to a number of first level vias in the planarized surface;

depositing a barrier/adhesion layer in the number of trenches using a low energy ion implantation of 100 to 700 electron volts;

depositing a seed layer on the barrier/adhesion layer in the number of trenches using a low energy ion implantation of 100 to 700 electron volts; and

depositing a metallic conductor over the seed layer.

10. The method of claim 9, wherein etching the insulator layer using a mask layer of photoresist to define a number of trenches in the insulator layer further includes:

leaving a residual photoresist layer on the insulator layer in a number of regions outside of the number of trenches; and

removing the barrier/adhesion layer and the seed layer from the number of regions outside of the number of trenches using a photoresist strip prior to depositing the metallic conductor over the seed layer.

11. The method of claim 9, wherein depositing a barrier/adhesion layer in the number of trenches includes depositing a barrier/adhesion layer of Zirconium using a low energy ion implantation of approximately 100 electron volts and using a varying angle implant, wherein an angle of implantation is changed from normal to the planarized surface to approximately 15 degrees off normal.

12. The method of claim 11, wherein depositing a barrier/adhesion layer of Zirconium includes depositing a barrier/adhesion layer of Zirconium having a thickness of approximately 50 Angstroms.

13. The method of claim 9, wherein depositing an insulator layer having a thickness suitable for a first level metal interconnect includes depositing a layer of polyimide having a thickness of approximately 5000 Angstroms.

14. The method of claim 9, wherein depositing a seed layer on the barrier/adhesion layer in the number of trenches includes depositing a layer of Copper using a low energy ion implantation of approximately 100 electron volts normal to the planarized surface.

15. The method of claim 14, wherein depositing a layer of Copper includes depositing a layer of Copper having a thickness of approximately 100 Angstroms.

16. The method of claim 15, wherein the method further includes depositing a layer of Aluminum having a thickness of approximately 50 Angstroms on the layer of Copper using a low energy ion implantation of approximately 100 electron volts normal to the planarized surface.

17. A method of making a diffusion barrier and a seed layer in an integrated circuit assembly, comprising:

depositing an insulator layer having a thickness suitable for a first level metal interconnect over a planarized surface;

etching the insulator layer using a mask layer of photoresist to define a number of trenches in the insulator layer opening to a number of first level vias in the planarized surface;

depositing a barrier/adhesion layer in the number of trenches having a thickness in the range of 5 to 150 Angstroms using a low energy ion implantation of 100 to 700 electron volts;

depositing a seed layer on the barrier/adhesion layer in the number of trenches having a thickness in the range of 5 to 150 Angstroms using a low energy ion implantation of 100 to 700 electron volts; and

depositing a metallic conductor over the seed layer using a selective deposition process.

18. The method of claim 17, wherein depositing an insulator layer includes depositing an oxide layer.

19. The method of claim 18, wherein depositing an oxide layer includes depositing a fluorinated silicon oxide.

20. The method of claim 17, wherein depositing a barrier/adhesion layer in the number of trenches includes depositing a barrier/adhesion layer of Titanium or Zirconium having a thickness of approximately 50 Angstroms and using a low energy ion implantation of approximately 100 electron volts.

21. The method of claim 17, wherein depositing a seed layer on the barrier/adhesion layer in the number of trenches includes:

depositing a first layer of Aluminum on the barrier/adhesion layer having a thickness of approximately 50 Angstroms using a low energy ion implantation of approximately 100 electron volts;

depositing a layer of Copper on the first layer of Aluminum having a thickness of approximately 10 Angstroms using a low energy ion implantation of approximately 100 electron volts; and

depositing a second layer of Aluminum on the layer of Copper having a thickness of approximately 50 Angstroms using a low energy ion implantation of approximately 100 electron volts.

22. The method of claim 21, wherein depositing a metallic conductor over the seed layer using a selective deposition process includes depositing a metallic conductor over the seed layer sufficient to fill the number of trenches to a top surface of the insulator layer.

implantation of approximately 100 electron volts includes implanting the seed layer of copper at an angle normal to the planarized surface.

27. The method of claim 23, wherein etching the insulator layer using a mask layer of photoresist to define a number of trenches in the insulator layer further includes:

leaving a residual photoresist layer on the insulator layer in a number of regions outside of the number of trenches; and

removing the tantalum, Nitrogen and seed layer of copper from the number of regions outside of the number of trenches using a photoresist strip prior to depositing the metallic conductor over the seed layer.

28. The method of claim 23, wherein depositing a metallic conductor over the seed layer using a selective deposition process includes depositing a layer of copper using electroless plating.

29. The method of claim 28, wherein depositing a metallic conductor over the seed layer includes filling the number of trenches to a height (h) approximately 100 Angstroms lower than a top surface of the oxide layer.

30. The method of claim 29, wherein the method further includes depositing a layer of tantalum nitride having a thickness of approximately 100 Angstroms on the metallic conductor in the number of trenches.

31. A method of forming copper metal lines in an integrated circuit assembly, comprising:

depositing a polymer layer having a thickness suitable for a first level metal interconnect over a planarized surface;

etching the polymer layer using a mask layer of photoresist to define a number of trenches in the polymer layer opening to a number of first level vias in the planarized surface;

depositing a layer of zirconium in the number of trenches, wherein the layer of zirconium has a thickness of approximately 15 Angstroms and is

deposited using a low energy ion implantation of approximately 100 electron volts;

depositing a seed layer of Copper on the layer of zirconium in the number of trenches having a thickness of approximately 50 Angstroms using a low energy ion implantation of approximately 100 electron volts; and

depositing a first level metallic conductor over the seed layer using a selective deposition process.

32. The method of claim 31, wherein the method further includes depositing a layer of aluminum having a thickness of approximately 50 Angstroms on the seed layer of Copper using a low energy ion implantation of approximately 100 electron volts.

33. The method of claim 31, wherein etching the polymer layer using a mask layer of photoresist to define a number of trenches in the polymer layer further includes:

leaving a residual photoresist layer on the polymer layer in a number of regions outside of the number of trenches; and

removing the zirconium and the seed layer of copper from the number of regions outside of the number of trenches using a photoresist strip prior to depositing the first level metallic conductor over the seed layer.

34. The method of claim 31, wherein depositing a metallic conductor over the seed layer using a selective deposition process includes depositing a layer of copper using electroless plating to fill the number of trenches to a top surface of the polymer layer.

35. The method of claim 31, wherein depositing a polymer layer includes depositing a foamed polymer layer.

36. The method of claim 35, wherein the method further includes:

depositing a polymer layer having a thickness of approximately 10,000 Angstroms in which to form a number of second level vias and a second level metal interconnect over the first level metallic conductor;

etching the polymer layer using a mask layer of photoresist in a dual damascene process to define a number of second level vias and a number of second level metal trenches in the polymer layer opening to the first level metallic conductor;

depositing a layer of zirconium in the number of second level vias and a number of second level metal trenches, wherein the layer of zirconium has a thickness of approximately 15 Angstroms and is deposited using a low energy ion implantation of approximately 100 electron volts;

depositing a seed layer of Copper on the layer of zirconium in the number of second level vias and a number of second level metal trenches having a thickness of approximately 50 Angstroms using a low energy ion implantation of approximately 100 electron volts; and

depositing a layer of copper over the seed layer in the number of second level vias and a number of second level metal trenches using a selective deposition process.

37. The method of claim 36, wherein the method further includes depositing a layer of aluminum having a thickness of approximately 50 Angstroms on the seed layer of Copper using a low energy ion implantation of approximately 100 electron volts.

38. The method of claim 37, wherein depositing a layer of copper over the seed layer includes depositing a layer of copper over the seed layer using electroless plating.

39. The method of claim 38, wherein the method further includes removing each of the polymer layers using an O_2 plasma etch.

40. A method of making a multilayer wiring structure in an integrated circuit assembly, comprising:

patterning a first insulator layer using a mask layer of photoresist to define a number of first level metal line trenches in the first insulator layer opening to a number of first level vias in the planarized surface;

depositing a first barrier/adhesion layer in the number of first level metal line trenches having a thickness in the range of 5 to 150 Angstroms using a low energy ion implantation of 100 to 700 electron volts;

depositing a first seed layer on the barrier/adhesion layer in the number of first level metal line trenches having a thickness in the range of 5 to 150 Angstroms using a low energy ion implantation of 100 to 700 electron volts;

depositing a number of first level metal lines over the seed layer using a selective deposition process;

depositing a second insulator layer having a thickness of approximately 10,000 Angstroms in which to form a number of second level vias and a second level metal interconnect over the number of first level metal lines;

etching the second insulator layer using a mask layer of photoresist in a dual damascene process to define a number of second level vias and a number of second level metal trenches in the second insulator layer opening to the number of first level metal lines;

depositing a second barrier/adhesion layer in the number of second level vias and a number of second level metal trenches having a thickness in the range of 5 to 150 Angstroms using a low energy ion implantation of 100 to 700 electron volts;

depositing a second seed layer on the barrier/adhesion layer in the number of second level vias and a number of second level metal trenches having a thickness in the range of 5 to 150 Angstroms using a low energy ion implantation of 100 to 700 electron volts; and

depositing a metal conductor over the second seed layer in the number of second level vias and the number of second level metal trenches using a selective deposition process.

41. The method of claim 40, wherein patterning a first insulator layer and depositing a second insulator layer includes patterning a first insulator layer and depositing a second insulator layer of polyimide.

42. The method of claim 40, wherein depositing a first and a second barrier/adhesion layer includes depositing a first and a second barrier/adhesion layer selected from the group consisting of tantalum nitride, titanium, zirconium, and hafnium.

43. The method of claim 40, wherein depositing a number of first level metal lines and depositing a metal conductor over the second seed layer includes depositing a number of first level metal lines and depositing a metal conductor over the second seed layer which are selected from the group consisting of Aluminum, Copper, Silver, and Gold.

44. The method of claim 40, wherein depositing a number of first level metal lines and depositing a metal conductor over the second seed layer includes depositing a number of first level metal lines and depositing a metal conductor over the second seed layer using electroless plating.

45. The method of claim 40, wherein depositing a first and a second seed layer on the first and the second barrier/adhesion layer includes depositing a first and a second seed layer selected from the group consisting of Aluminum, Copper, Silver, and Gold.

46. The method of claim 40, wherein patterning a first insulator layer using a mask layer of photoresist and etching the second insulator layer using a mask layer of photoresist in a dual damascene process includes:

leaving a residual photoresist layer on a top surface of the first and the second insulator layers; and

removing the first and the second barrier/adhesion layers as well as the first and the second seed layers from above the top surface of the first and the second insulator layers using a photoresist strip prior to depositing the number of

first level metal lines and prior to depositing a metal conductor over the second seed layer.

47. A metal layer in an integrated circuit, comprising:

a number of first level vias connecting to a number of silicon devices in a substrate; and

a number of first level metal lines formed above and connecting to the number of first level vias;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level metal lines; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the number of first level metal lines.

48. The metal layer of claim 47, wherein the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms includes a barrier/adhesion layer selected from the group consisting of titanium, zirconium, and hafnium.

49. The metal layer of claim 47, wherein the number of first level vias connecting to a number of silicon devices in a substrate are surrounded by an insulator layer.

50. The metal layer of claim 47, wherein the barrier/adhesion layer formed on the number of first level metal lines is surrounded by a polyimide insulator layer.

51. The metal layer of claim 47, wherein the number of first level metal lines includes a number of first level metal lines is selected from the group consisting of Aluminum, Copper, Silver, and Gold.

52. An integrated memory circuit, comprising:

a substrate including one or more transistors;

an insulator layer overlying the substrate having one or more first level vias connecting to the one or more transistors in the substrate; and

a polyimide layer overlying the insulator layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a number of first level metal lines;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level metal lines; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the number of first level metal lines.

53. A system, comprising:

a processor; and

an integrated memory circuit coupled to the processor, wherein the integrated memory circuit further includes:

a substrate including one or more transistors;

an insulator layer overlying the substrate having one or more first level vias connecting to the one or more transistors in the substrate; and

a polyimide layer overlying the insulator layer including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a number of first level metal lines;

a barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms formed on the number of first level metal lines; and

a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the number of first level metal lines.

54. The system of claim 53, wherein the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms includes a barrier/adhesion layer selected from the group consisting of titanium, zirconium, and hafnium.

55. The system of claim 53, wherein the a seed layer having a thickness in the range of 5 to 150 Angstroms formed at least between a portion of the barrier/adhesion layer and the number of first level metal lines includes a copper seed layer, and the number of first level metal lines includes a number of copper metal lines.

56. A metal layer in an integrated circuit, comprising:

a number of first level vias in a first insulator layer connecting to a number of silicon devices in a substrate; and

an oxide layer formed over the number of first level vias in the first insulator layer, wherein the oxide layer includes a number of conductive structures connecting from a top surface of the oxide layer to the number of first level vias, each conductive structure, comprising:

a layer of Titanium or Zirconium having a thickness of approximately 50 Angstroms;

a first layer of Aluminum on the layer of Titanium or Zirconium having a thickness of approximately 50 Angstroms;

a layer of Copper on the first layer of Aluminum having a thickness of approximately 10 Angstroms; and

a second layer of Aluminum on the layer of Copper having a thickness of approximately 50 Angstroms.

57. A metal interconnect in an integrated circuit, comprising:

a number of first level vias in a first insulator layer connecting to a number of silicon devices in a substrate; and

an oxide layer formed over the number of first level vias in the first insulator layer, wherein the oxide layer includes a number of conductive structures connecting from a top surface of the oxide layer to the number of first level vias, each conductive structure, comprising:

a layer of tantalum having a thickness of approximately 100 Angstroms;

a layer of Nitrogen on the layer of tantalum;

a seed layer of Copper on layer of Nitrogen having a thickness of approximately 100 Angstroms; and

a copper metal line formed on the seed layer of copper.

58. The metal layer of claim 57, wherein each conductive structure further includes a layer of tantalum nitride forming a top surface of each conductive structure such that the top surface of each conductive structure is level with the top surface of the oxide layer.

59. A wiring structure in an integrated circuit, comprising:

a number of first level vias in a first insulator layer connecting to a number of silicon devices in a substrate; and

a first number of conductive structures formed over and connecting to the number of first level vias in the first insulator layer, each conductive structure, comprising:

a layer of zirconium having a thickness of approximately 15 Angstroms;

a seed layer of copper on the layer of zirconium having a thickness of approximately 50 Angstroms; and

a copper metal line formed on the seed layer of copper.

60. The wiring structure of claim 59, wherein each conductive structure further includes a layer of aluminum having a thickness of approximately 50 Angstroms formed between the seed layer of copper and the copper metal line.

61. The wiring structure of claim 59, wherein the wiring structure further includes a polymer layer surrounding the number of conductive structures.

62. The wiring structure of claim 61, wherein the polymer layer includes a foamed polymer layer.

63. The wiring structure of claim 59, wherein the wiring structure further includes:

a second number of conductive structures including a number of second level vias and a number of second level metal lines formed above and connecting to the first number of conductive structures, wherein each of the second number of conductive structures includes:

a layer of zirconium having a thickness of approximately 15 Angstroms;

a seed layer of copper on at least a portion of the layer of zirconium having a thickness of approximately 50 Angstroms; and

a core copper conductor over the seed layer and within the layer of zirconium.

64. A multilayer wiring structure in an integrated circuit assembly, comprising:

a number of first level vias in a first insulator layer connecting to a number of silicon devices in a substrate;

a first number of conductive structures formed over and connecting to the number of first level vias in the first insulator layer, each conductive structure, comprising:

a first barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms;

a first seed layer formed on at least a portion of the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms; and

a first core conductor formed on the first seed layer and within the first barrier/adhesion layer; and

a second number of conductive structures includes a number of second level vias and a number of second level metal lines, wherein the second number of conductive structures are formed over and connect to the first number of conductive structures, and wherein each of the second number of conductive structures includes:

a second barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms;

a second seed layer formed on at least a portion of the barrier/adhesion layer having a thickness in the range of 5 to 150 Angstroms; and

a second core conductor formed on the second seed layer and within the second barrier/adhesion layer.

65. The multilayer wiring structure of claim 64, wherein the first and the second number of conductors are surrounded by a polyimide layer.

66. The multilayer wiring structure of claim 64, wherein the polyimide layer includes a foamed polyimide layer.

67. The multilayer wiring structure of claim 64, wherein the first and the second barrier/adhesion layers include a first and a second barrier/adhesion layer selected from the group consisting of tantalum nitride, titanium, zirconium, and hafnium.

68. The multilayer wiring structure of claim 64, wherein the first and the second core conductors include a metal conductor selected from the group consisting of Aluminum, Copper, Silver, and Gold.

69. The multilayer wiring structure of claim 64, wherein the first and the second seed layers include a first and a second seed layer selected from the group consisting of Aluminum, Copper, Silver, and Gold.

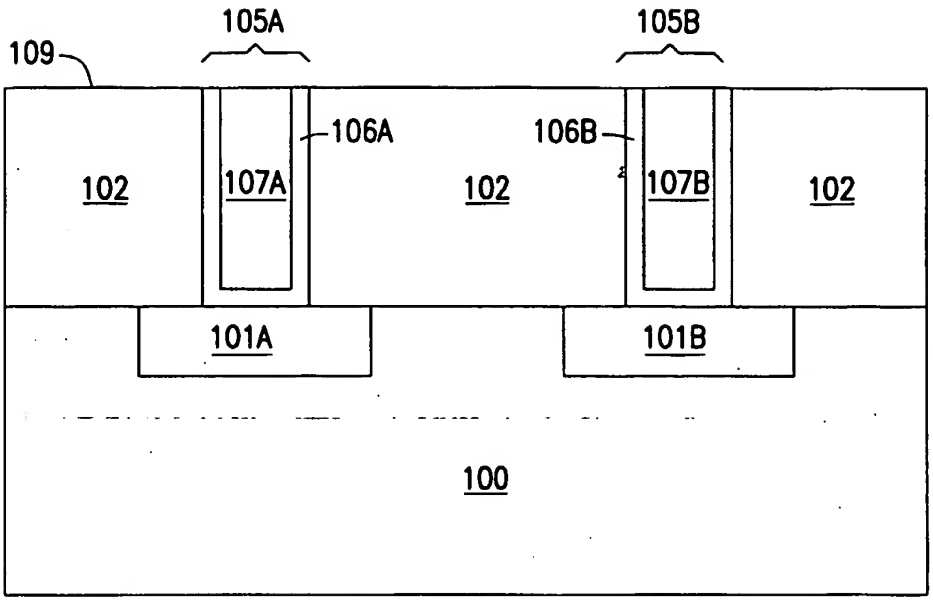

FIG. 1A

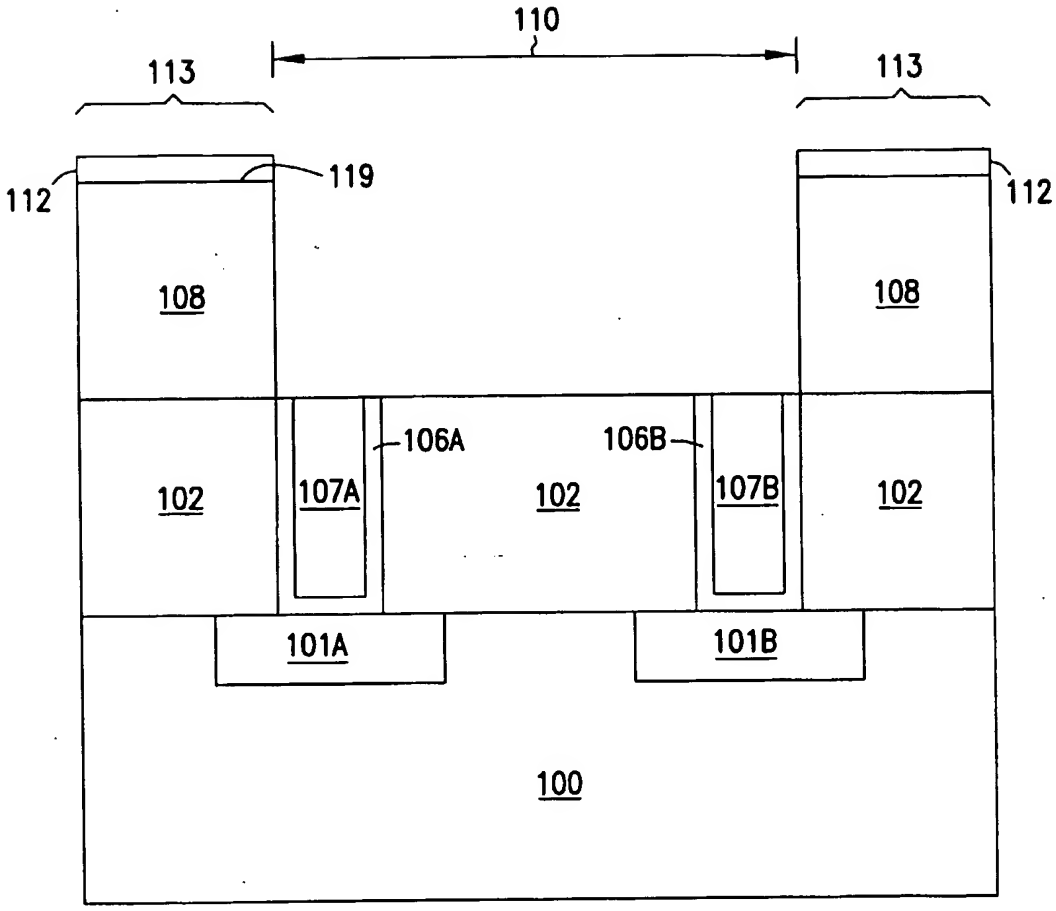
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FIG. 1B

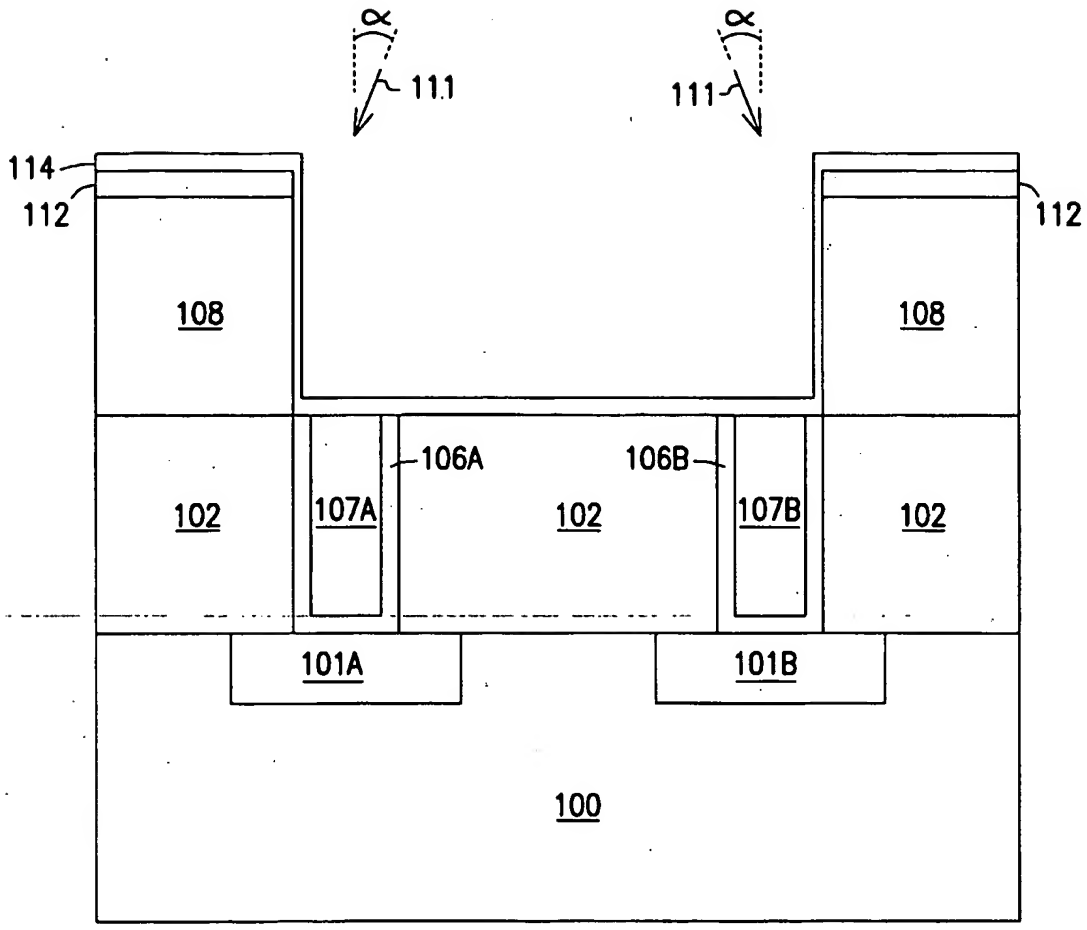
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FIG. 1C

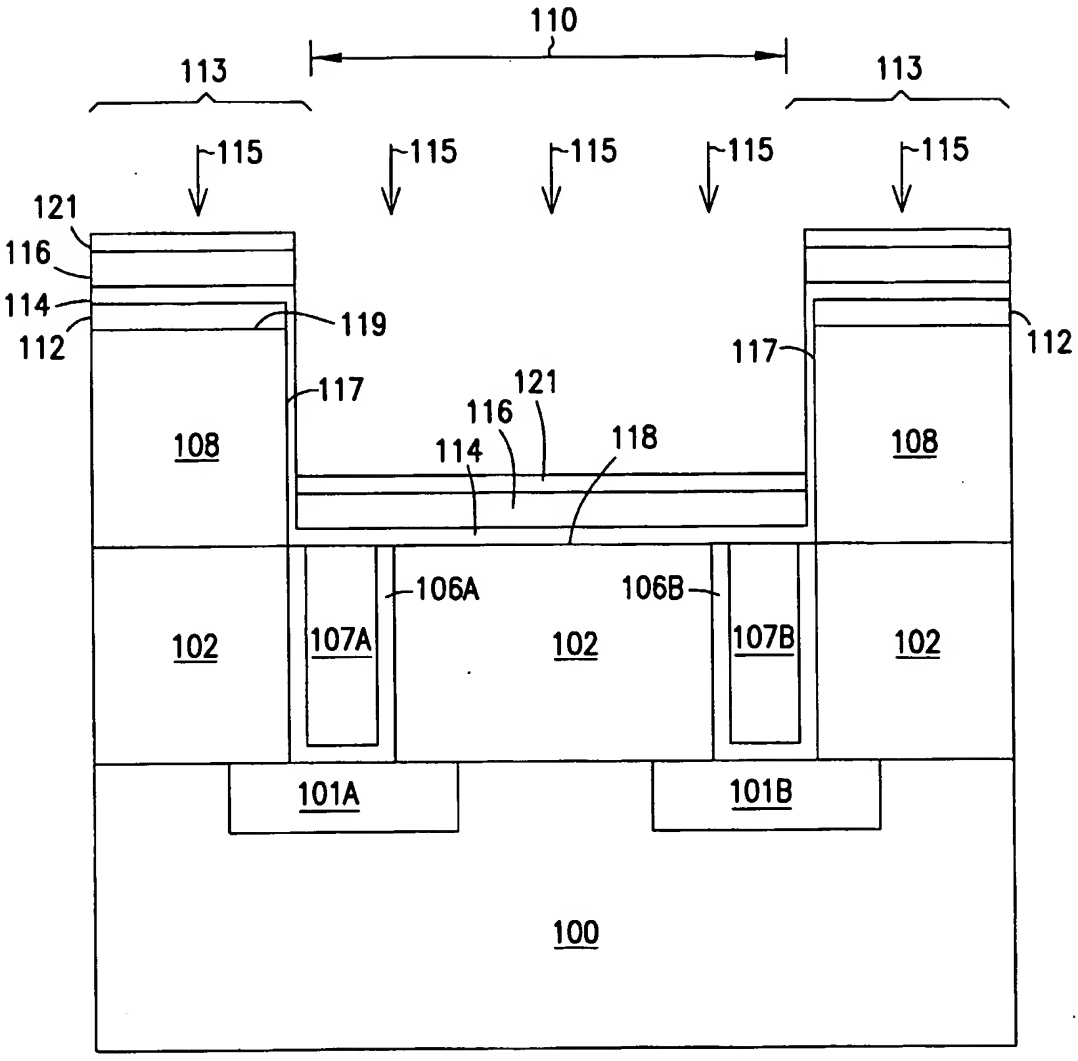
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FIG. 1D

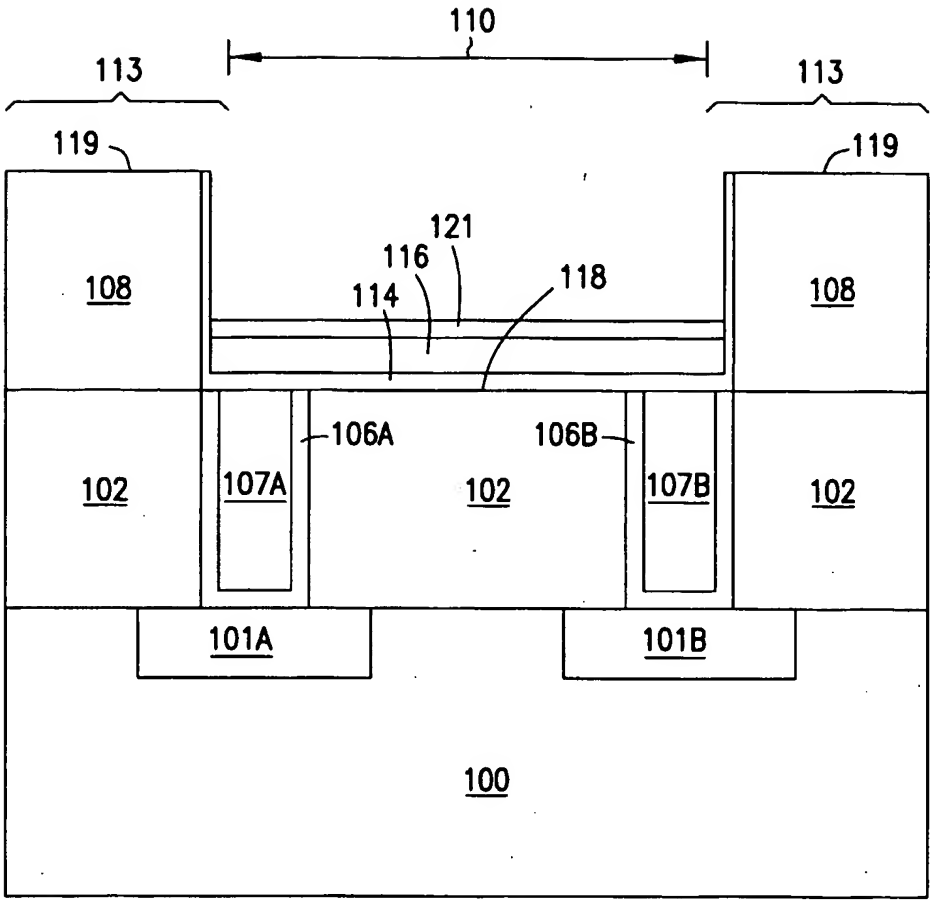
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FIG. 1E

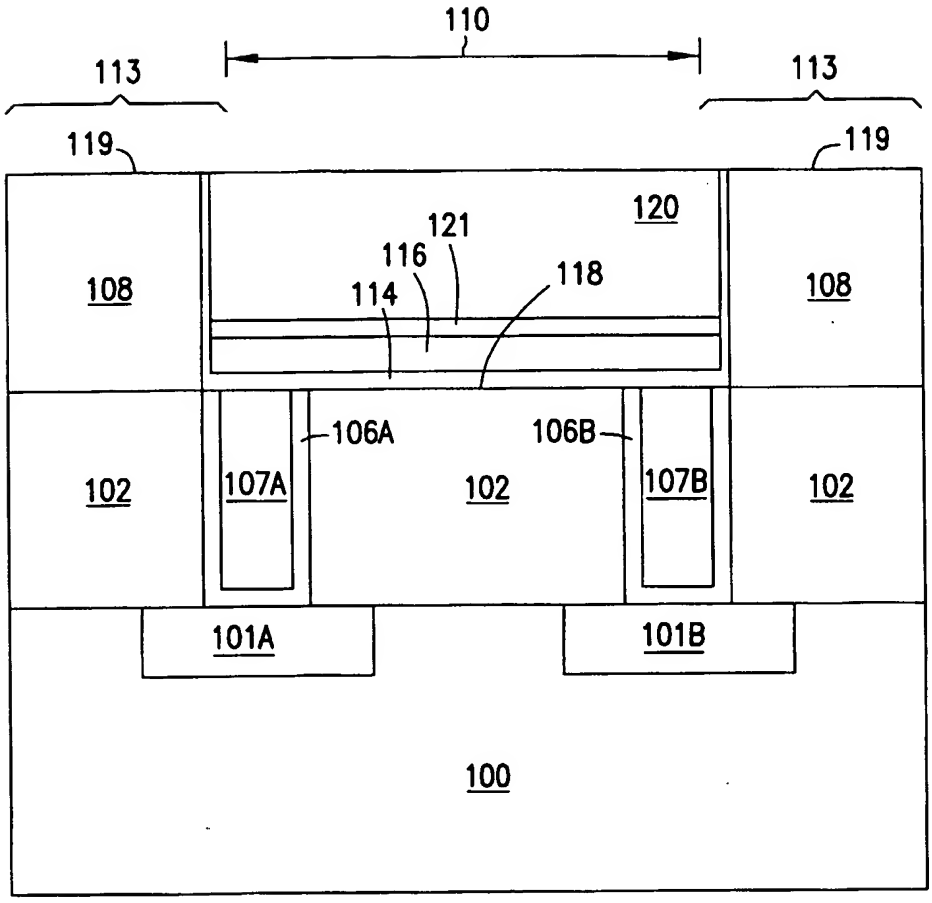
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FIG. 1F

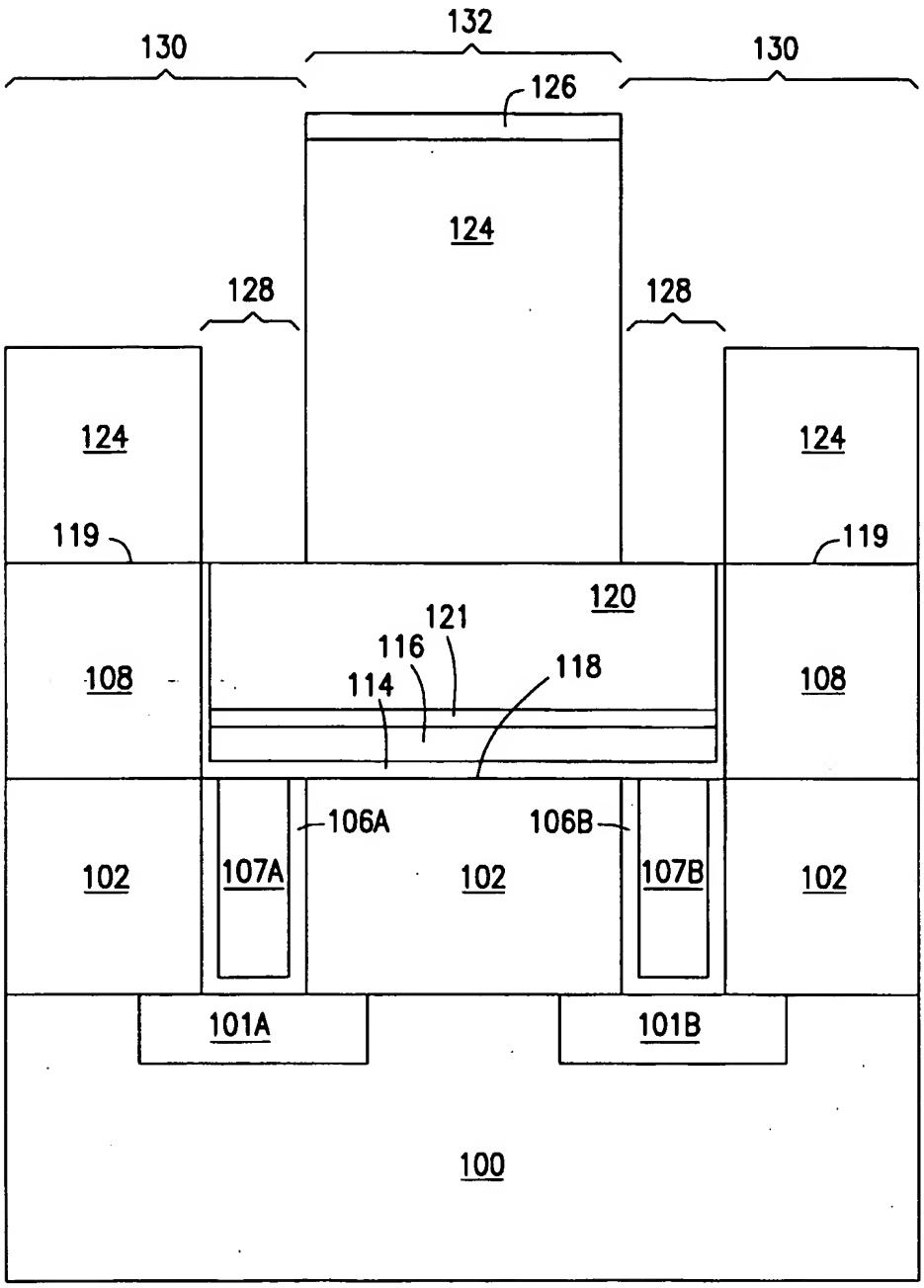
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FIG. 1G

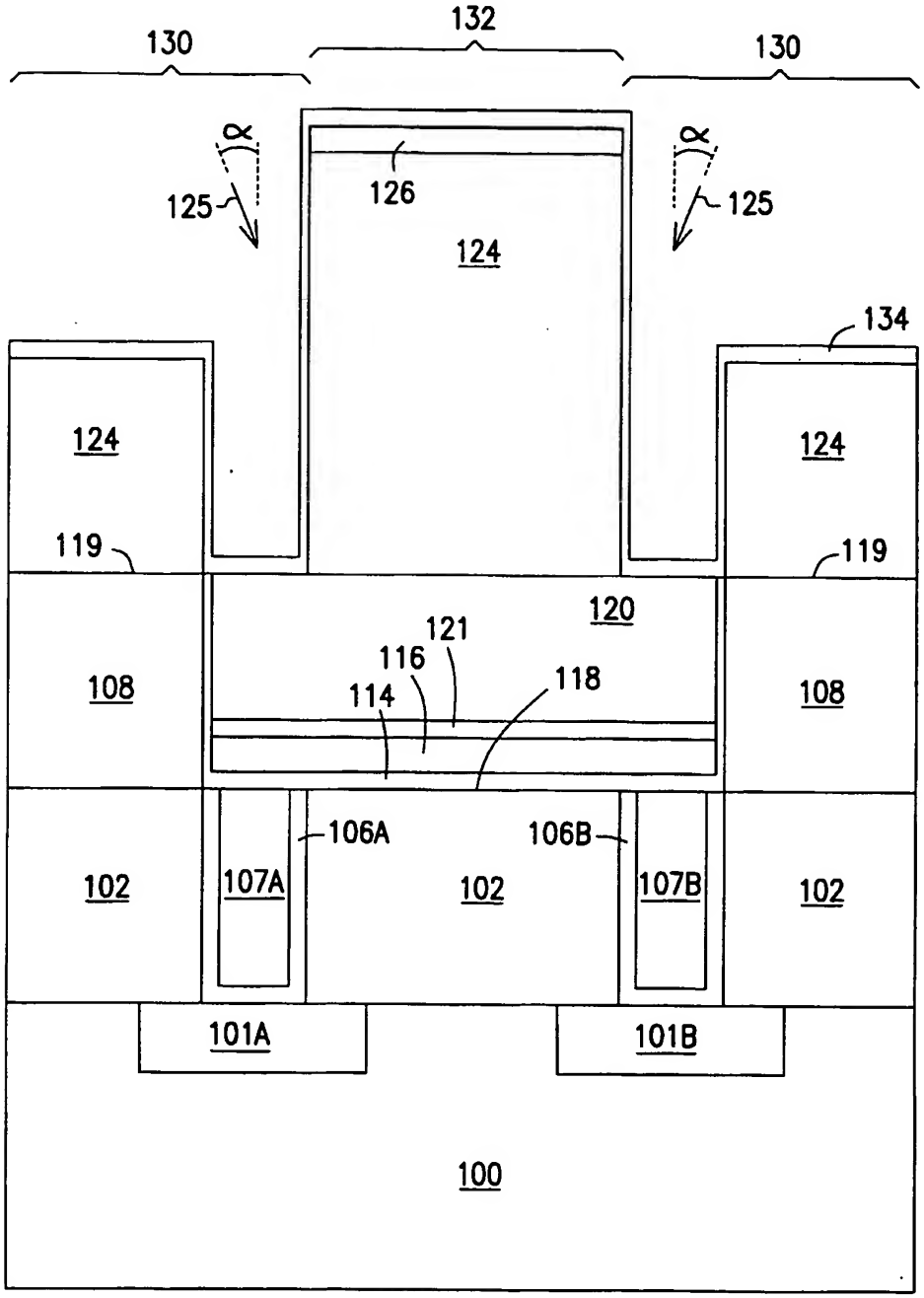
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FIG. 1H

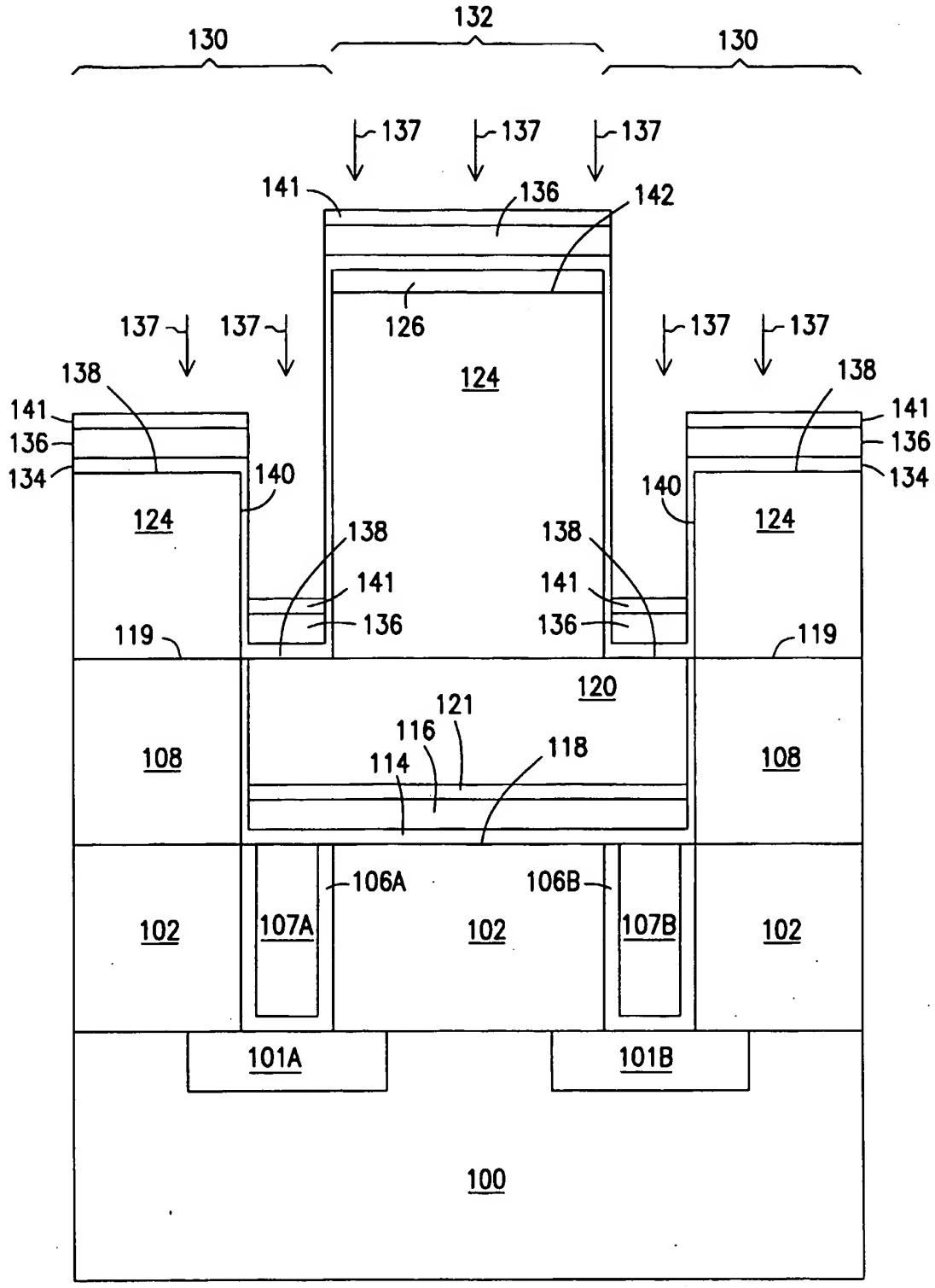
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FIG. 11

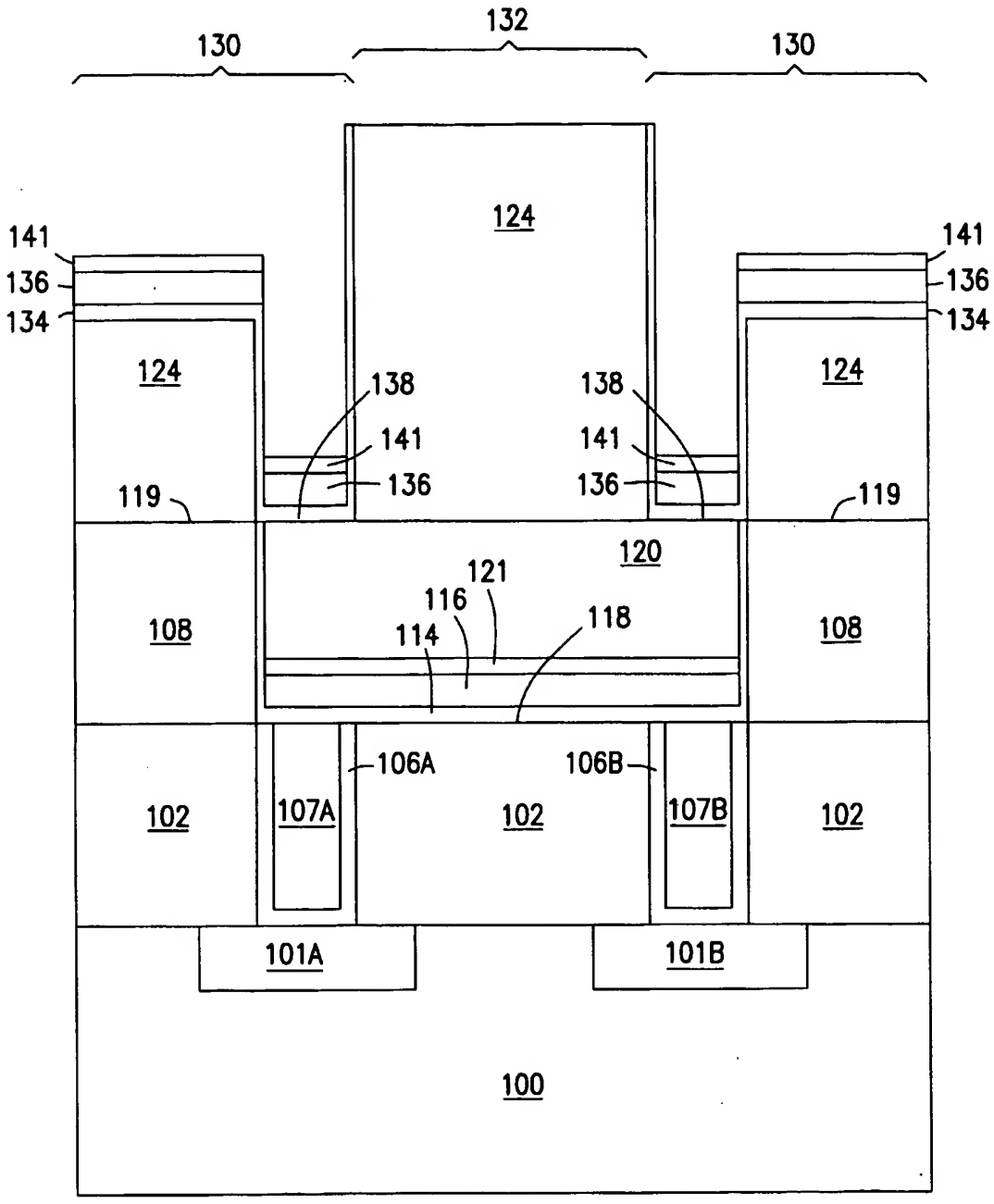
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FIG. 1J

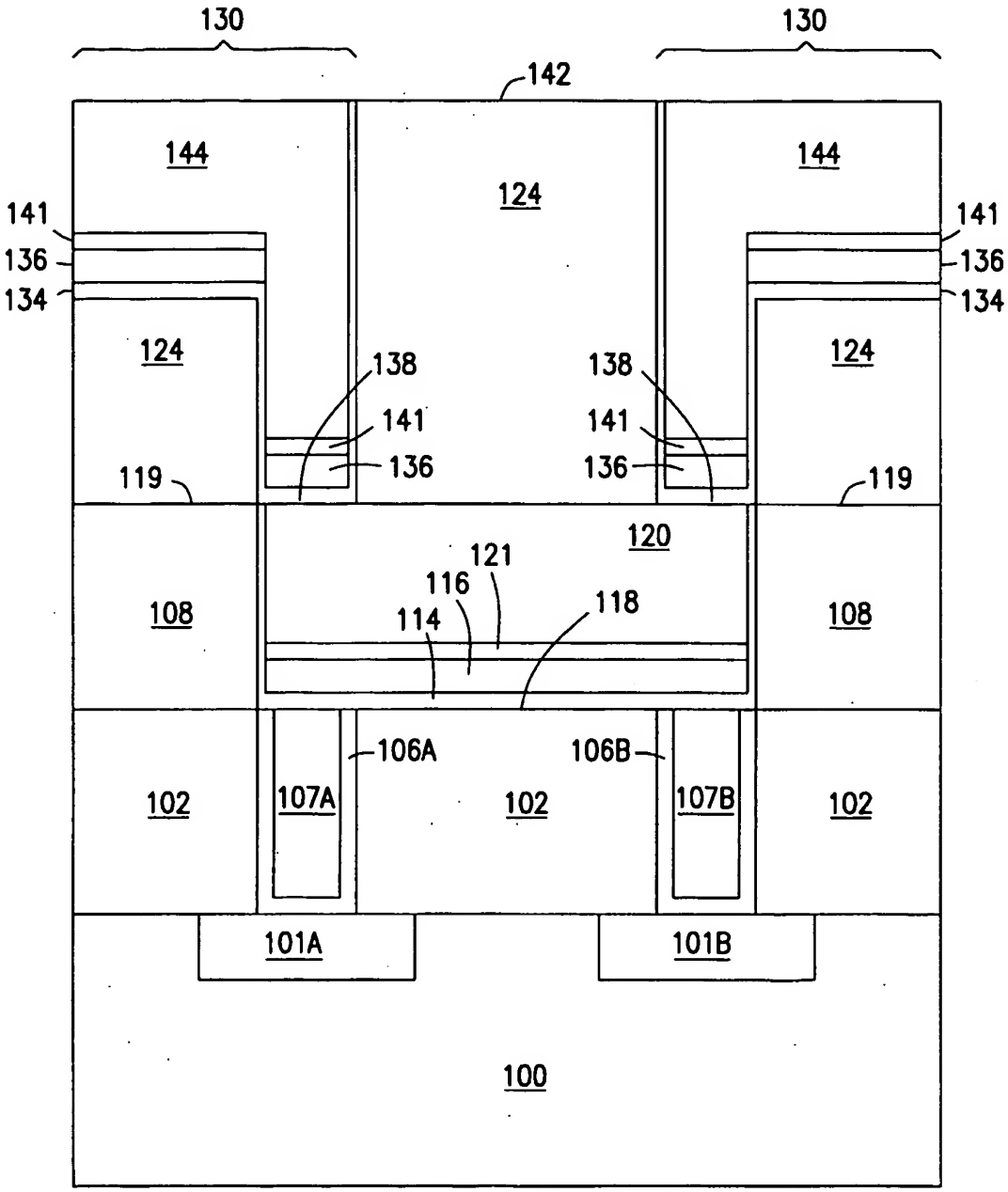
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FIG. 1K

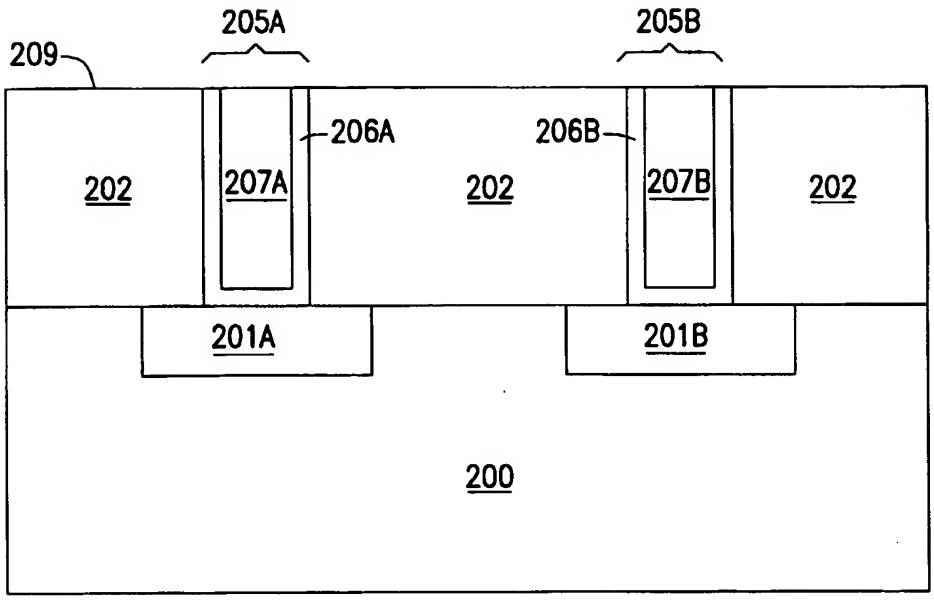

FIG. 2A

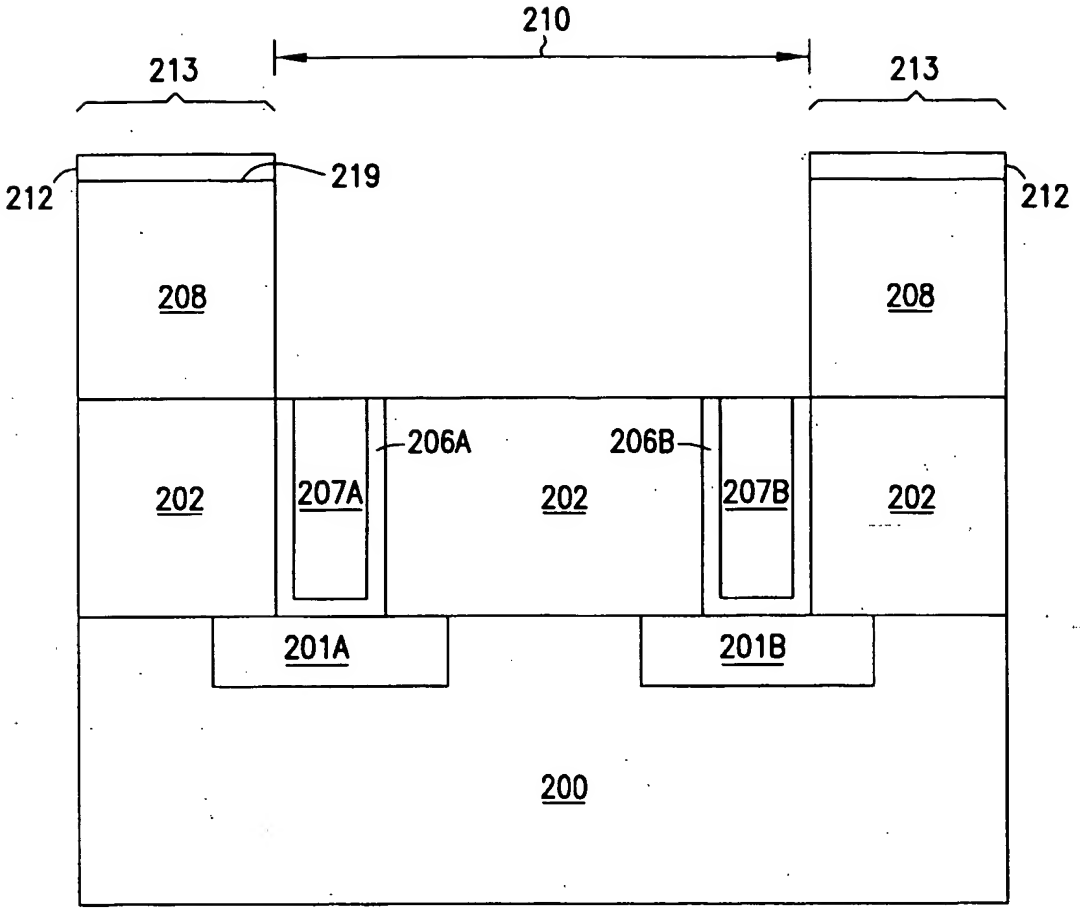
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FIG. 2B

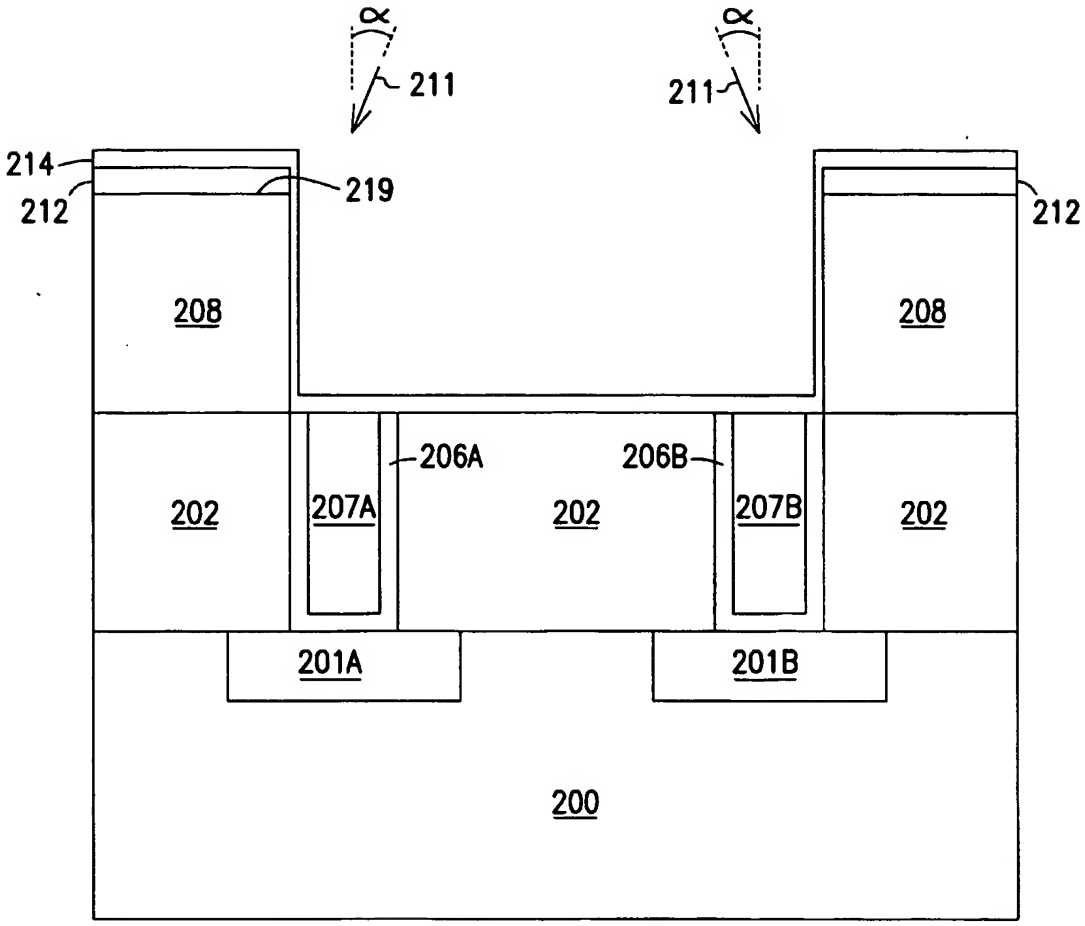
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FIG. 2C

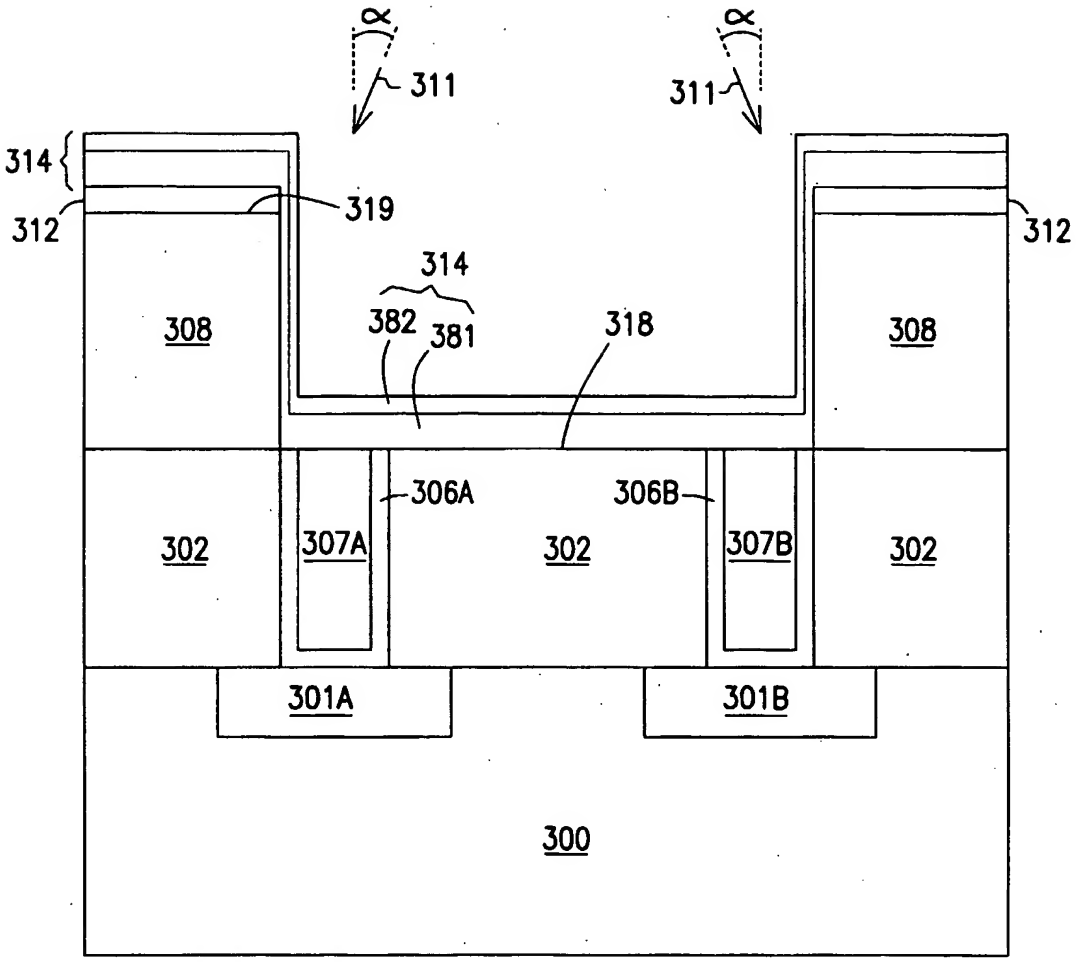
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FIG. 3C

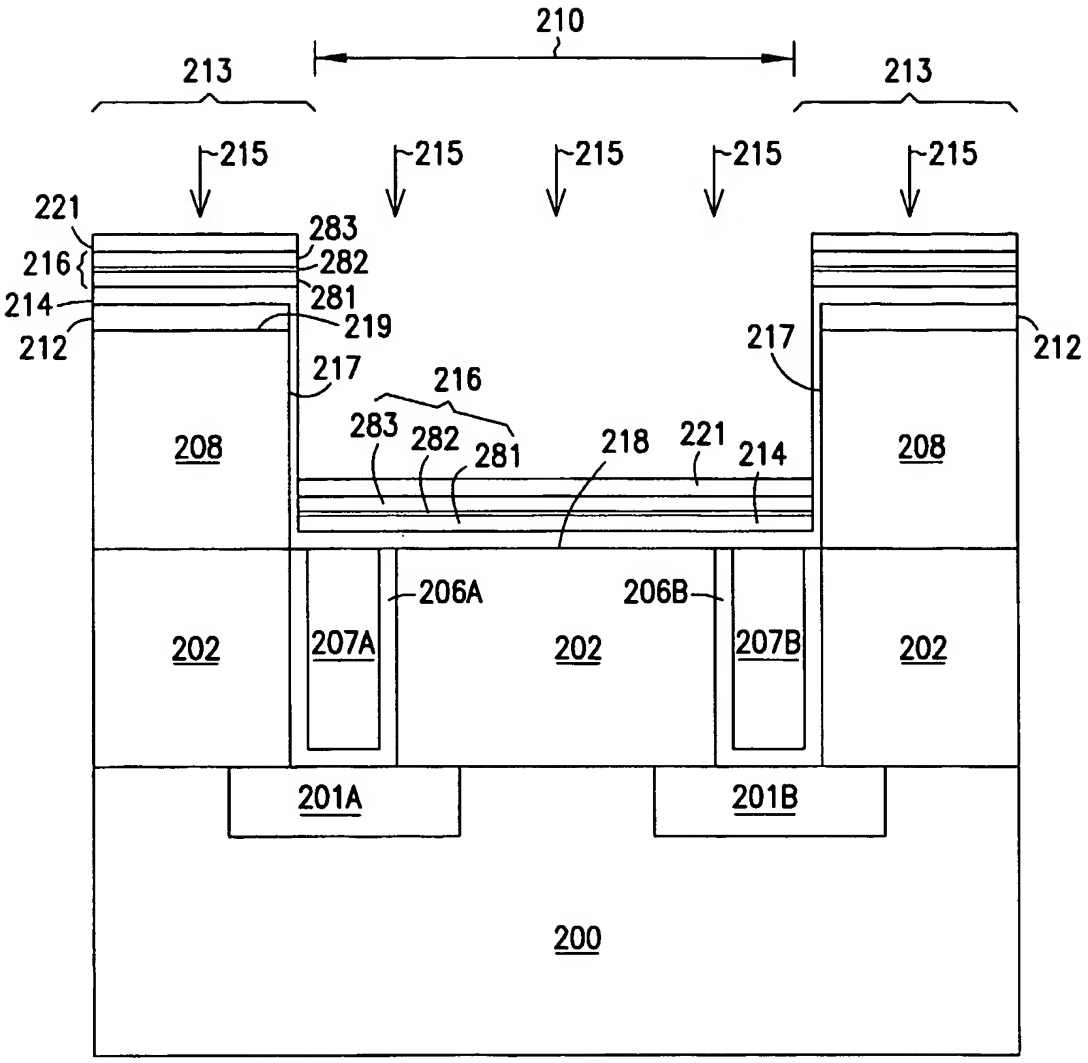
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FIG. 2D

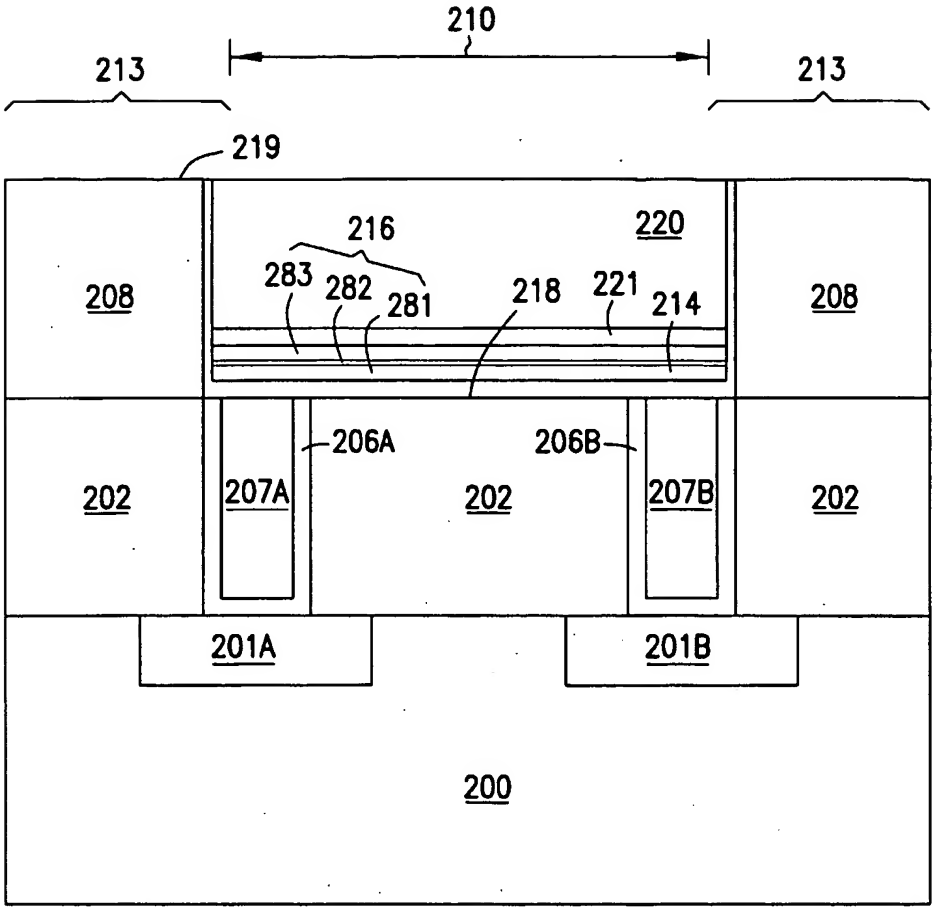
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FIG. 2E

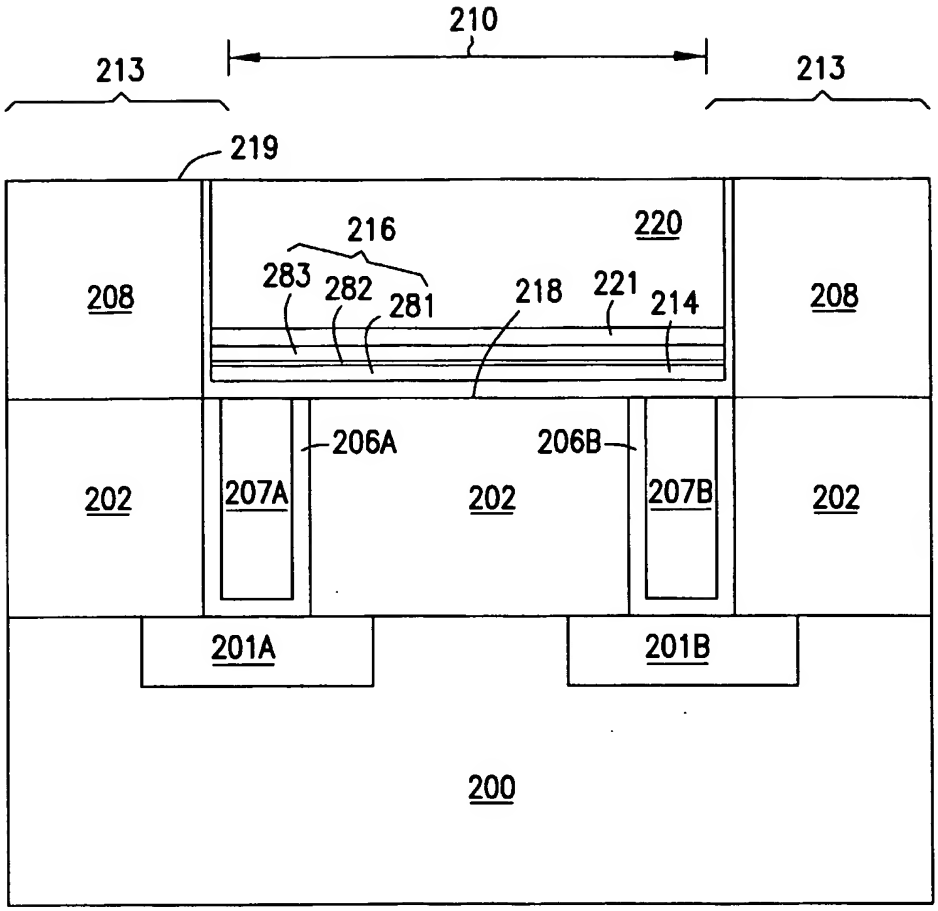
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FIG. 2F

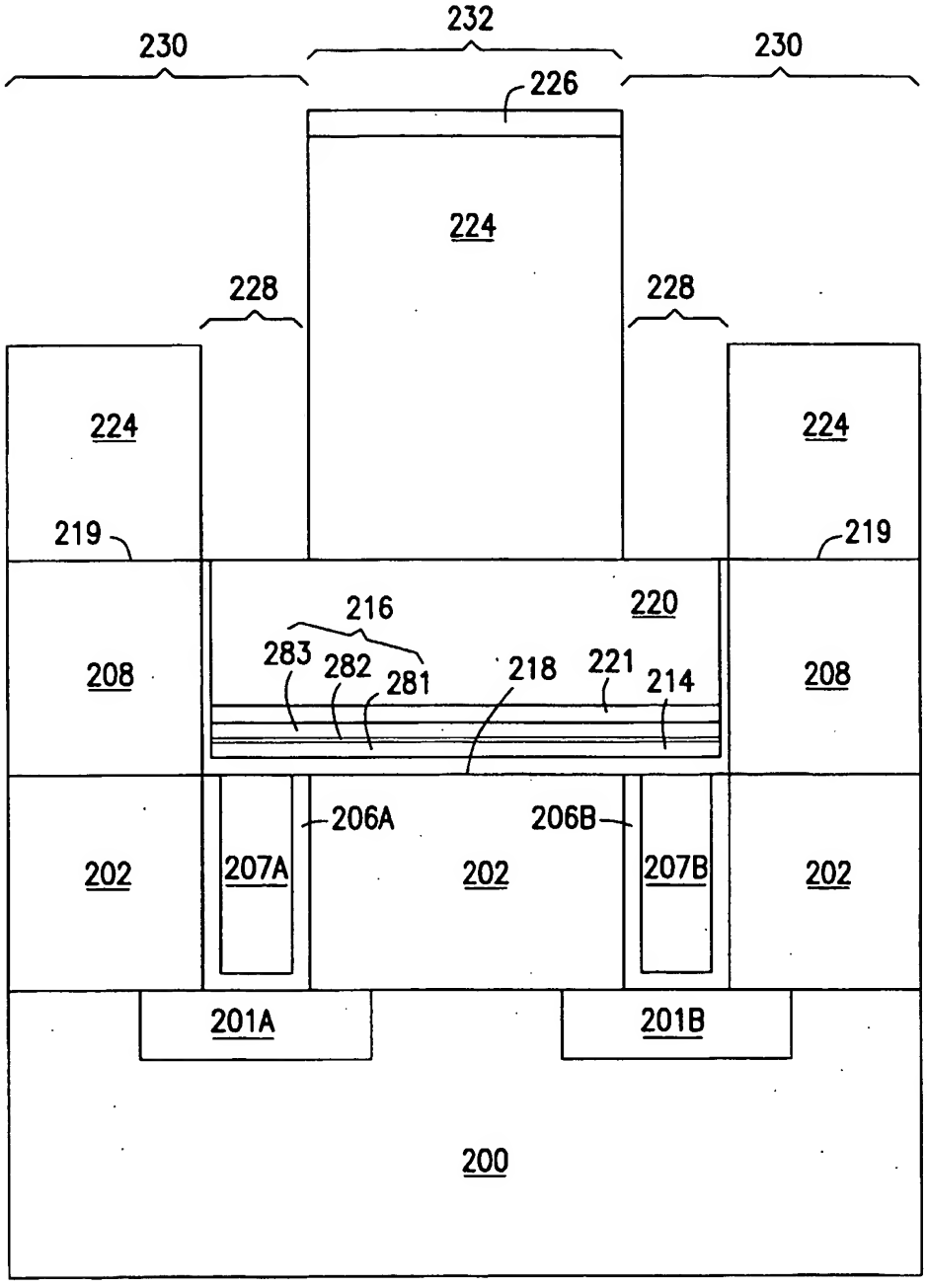
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FIG. 2G

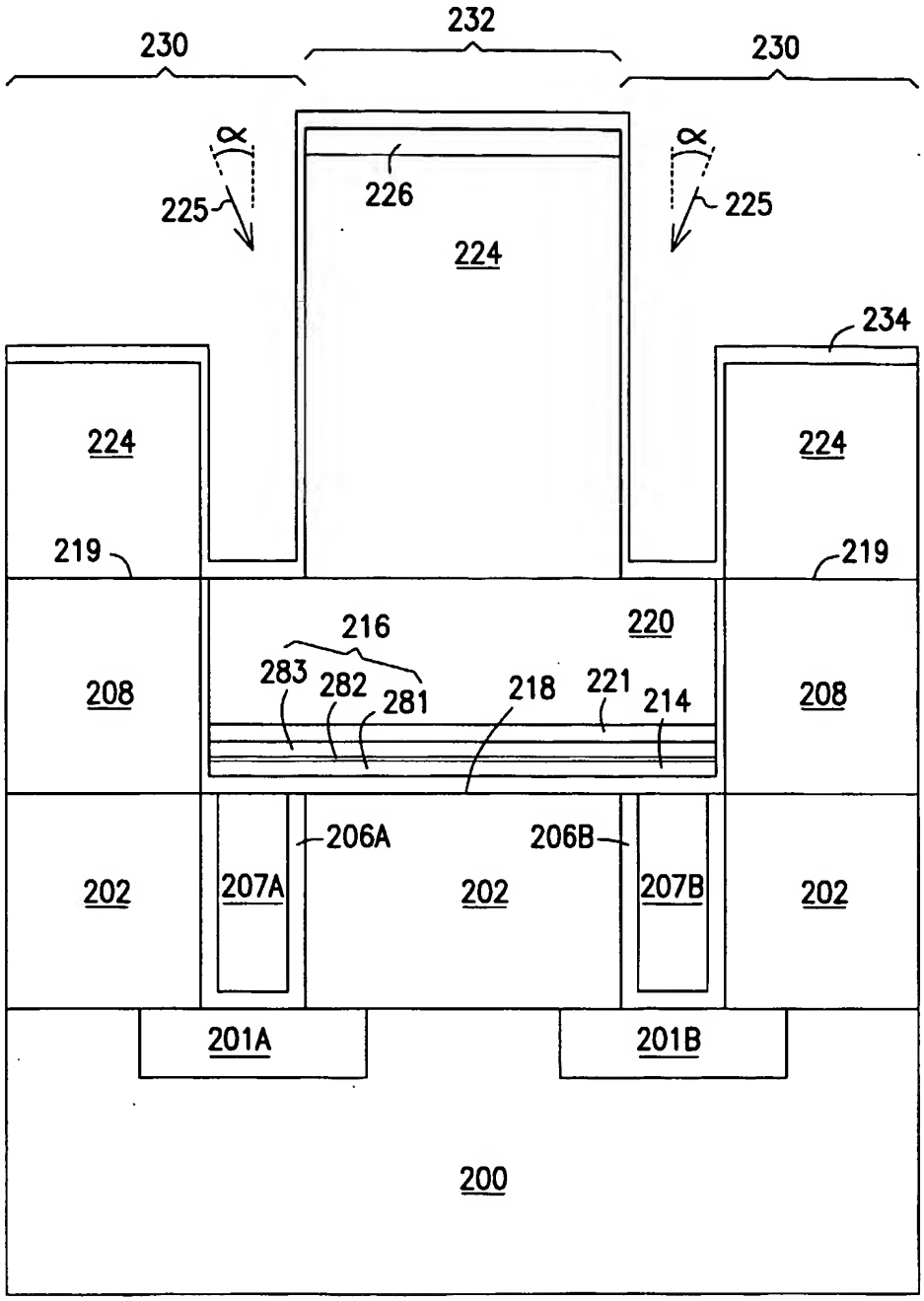
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FIG. 2H

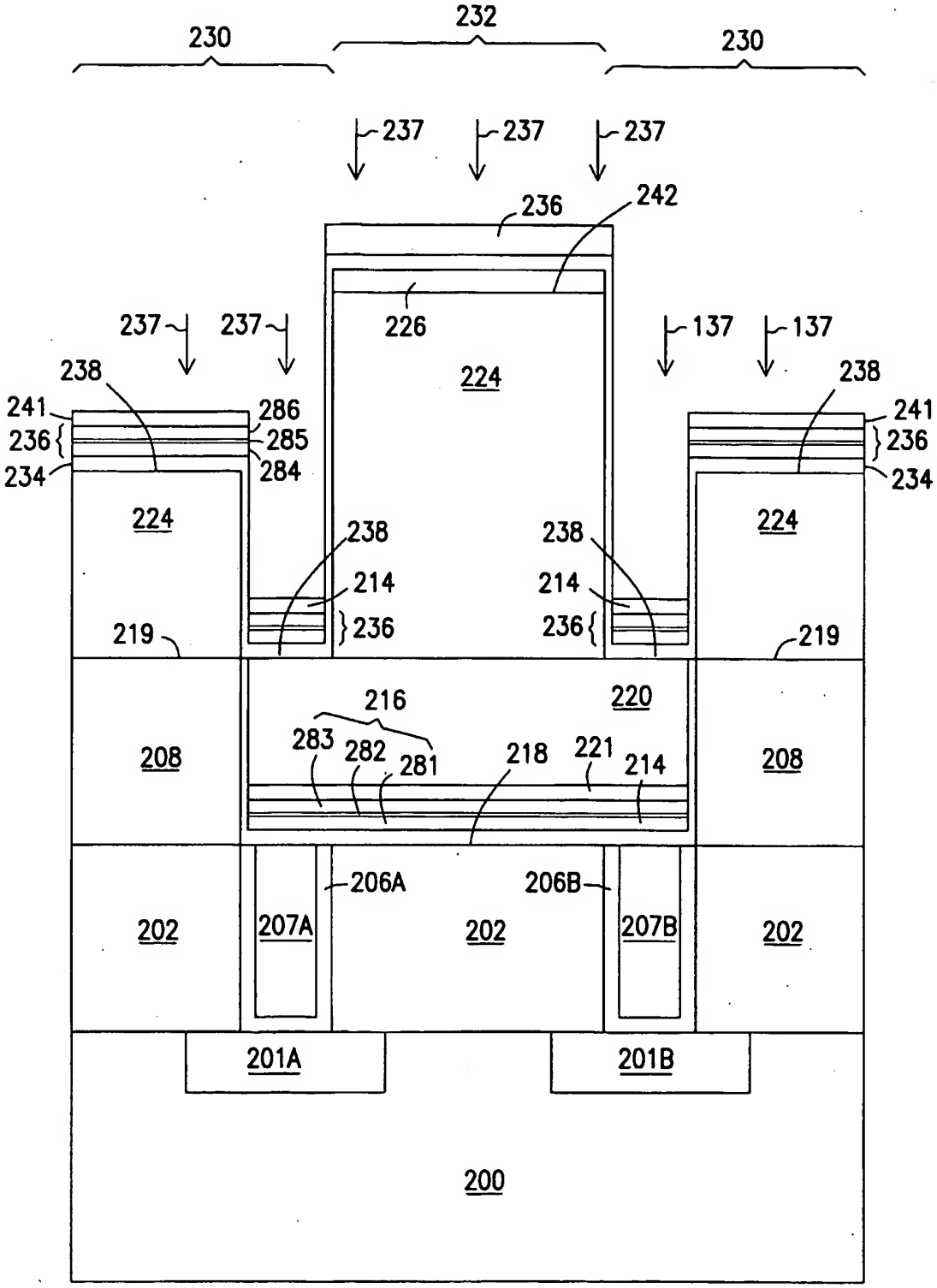
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FIG. 21

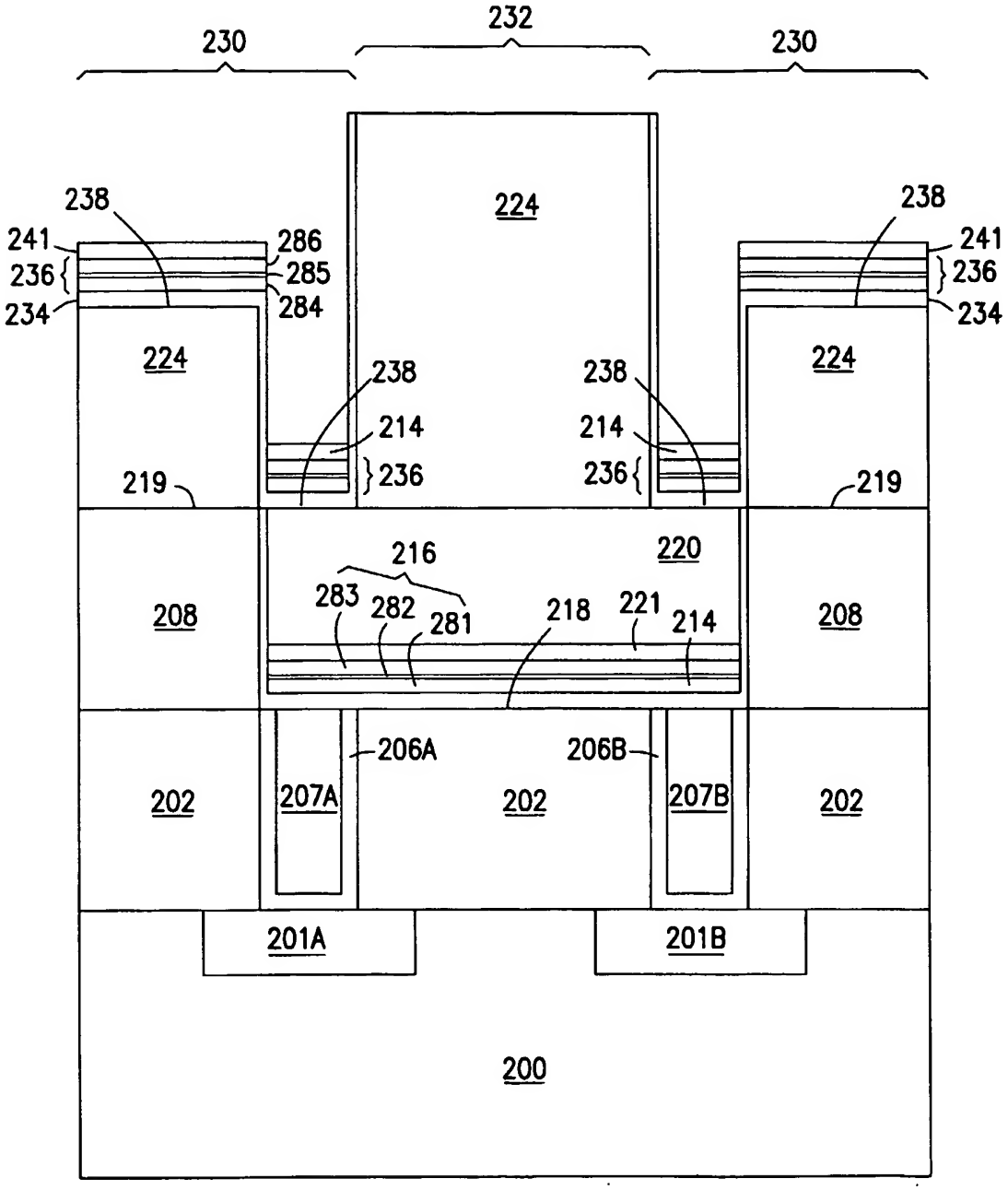
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FIG. 2J

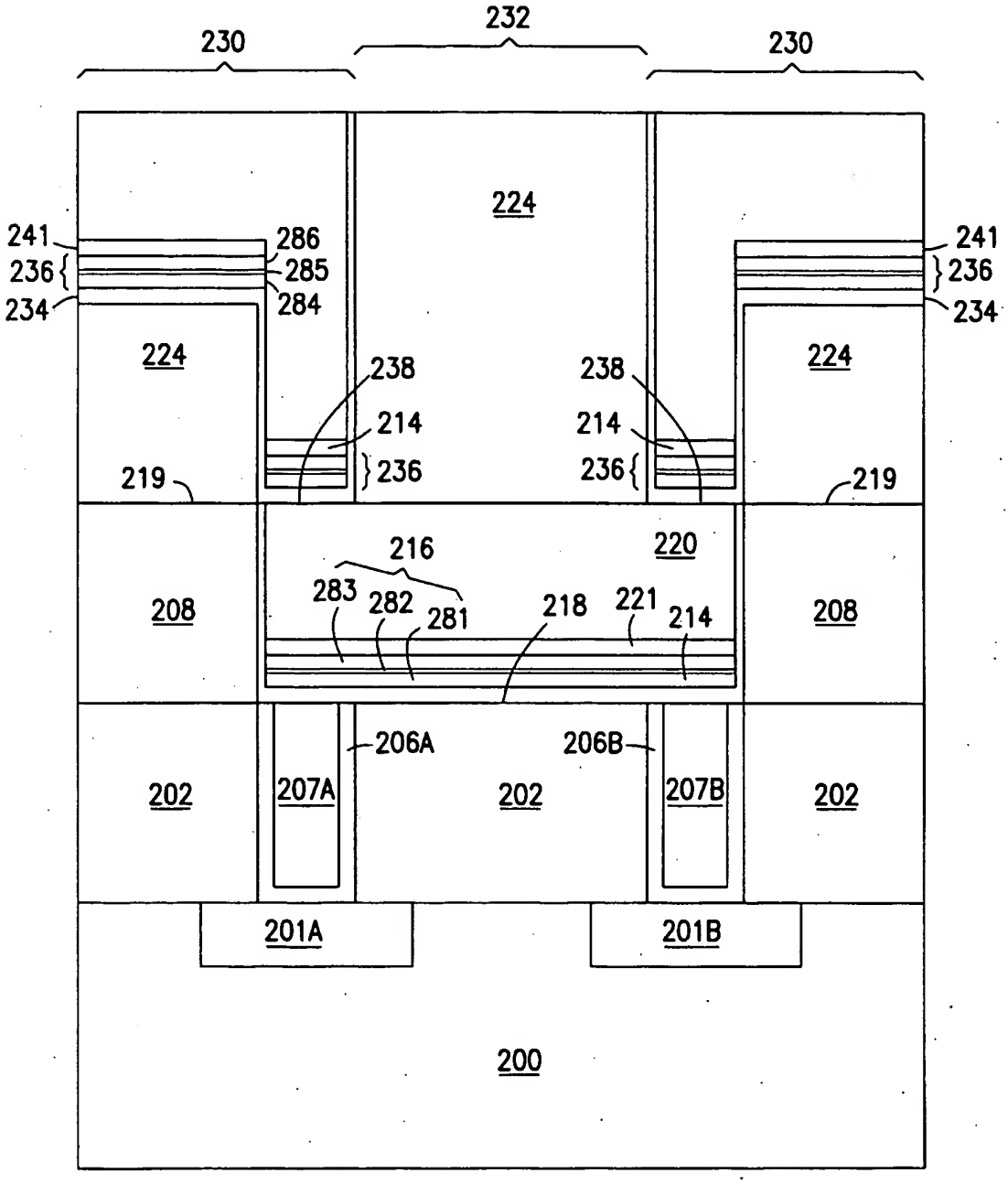
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FIG. 2K

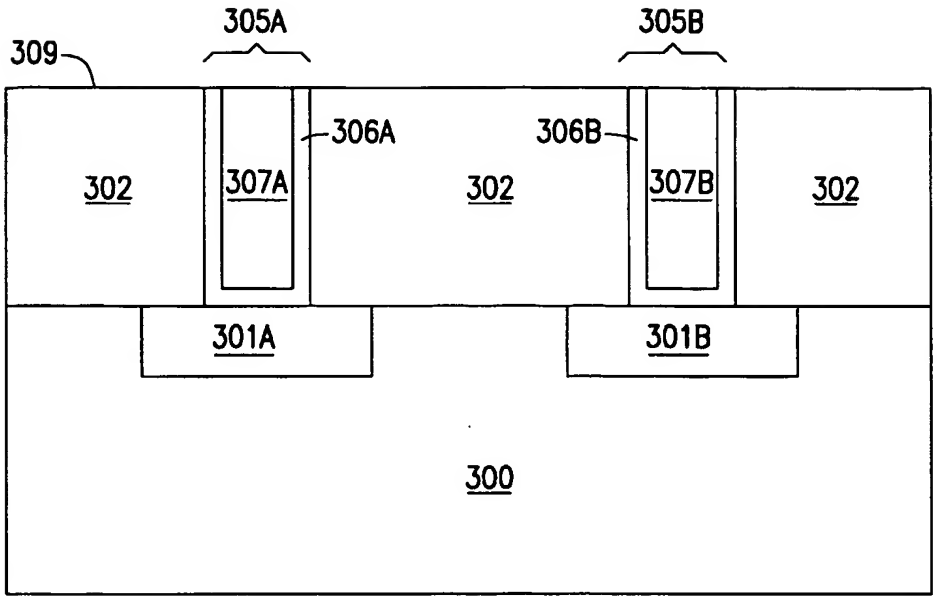

FIG. 3A

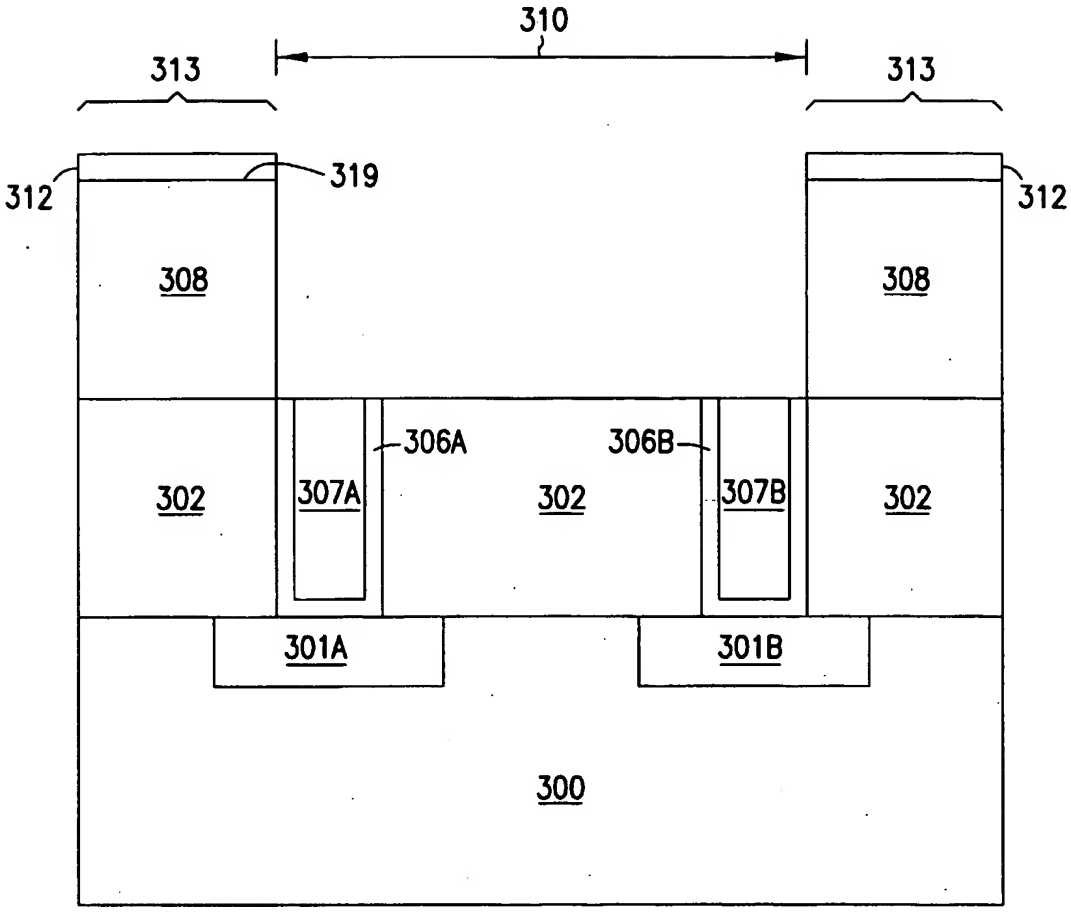
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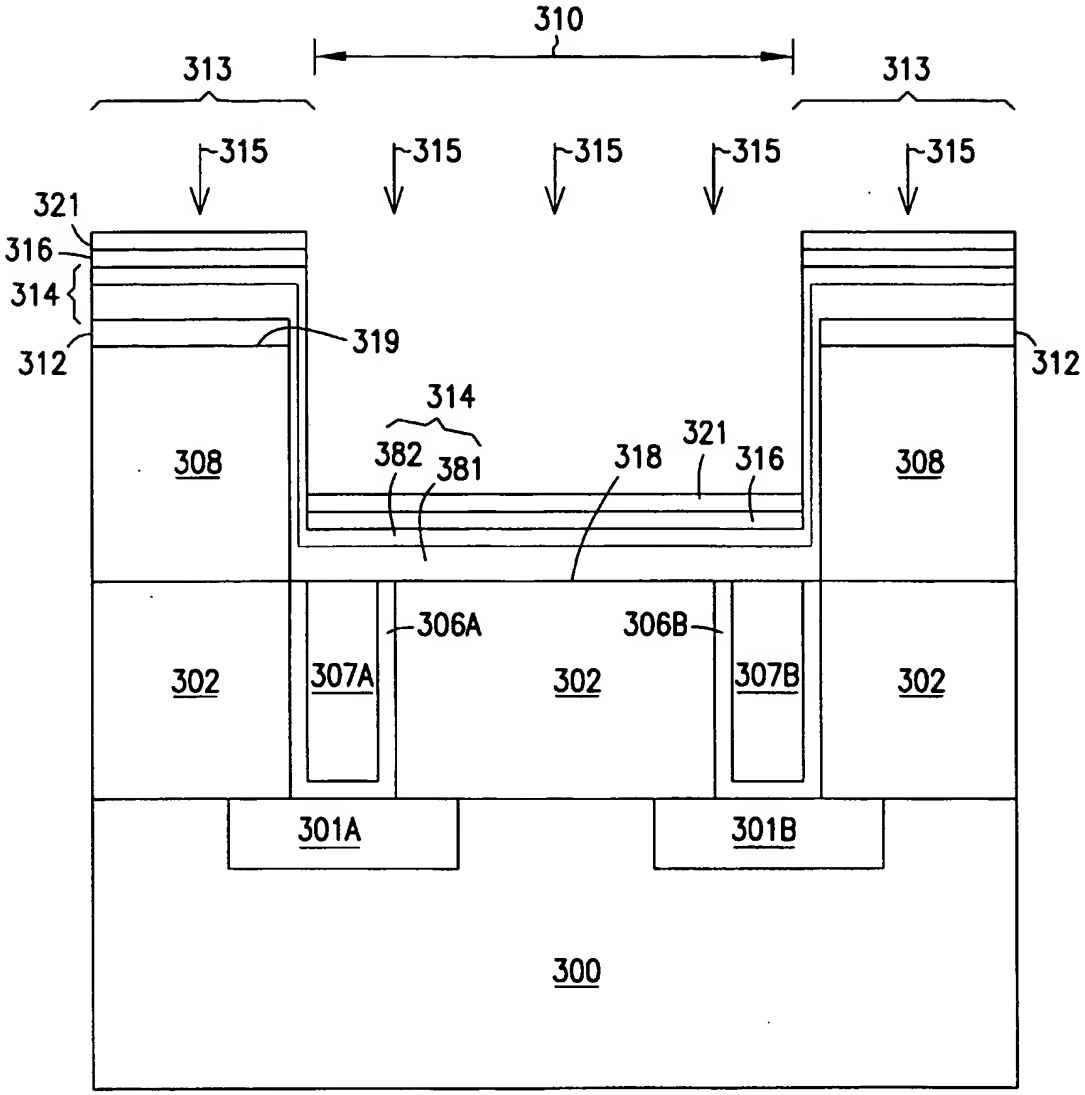
FIG. 3B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301A
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FIG. 3D

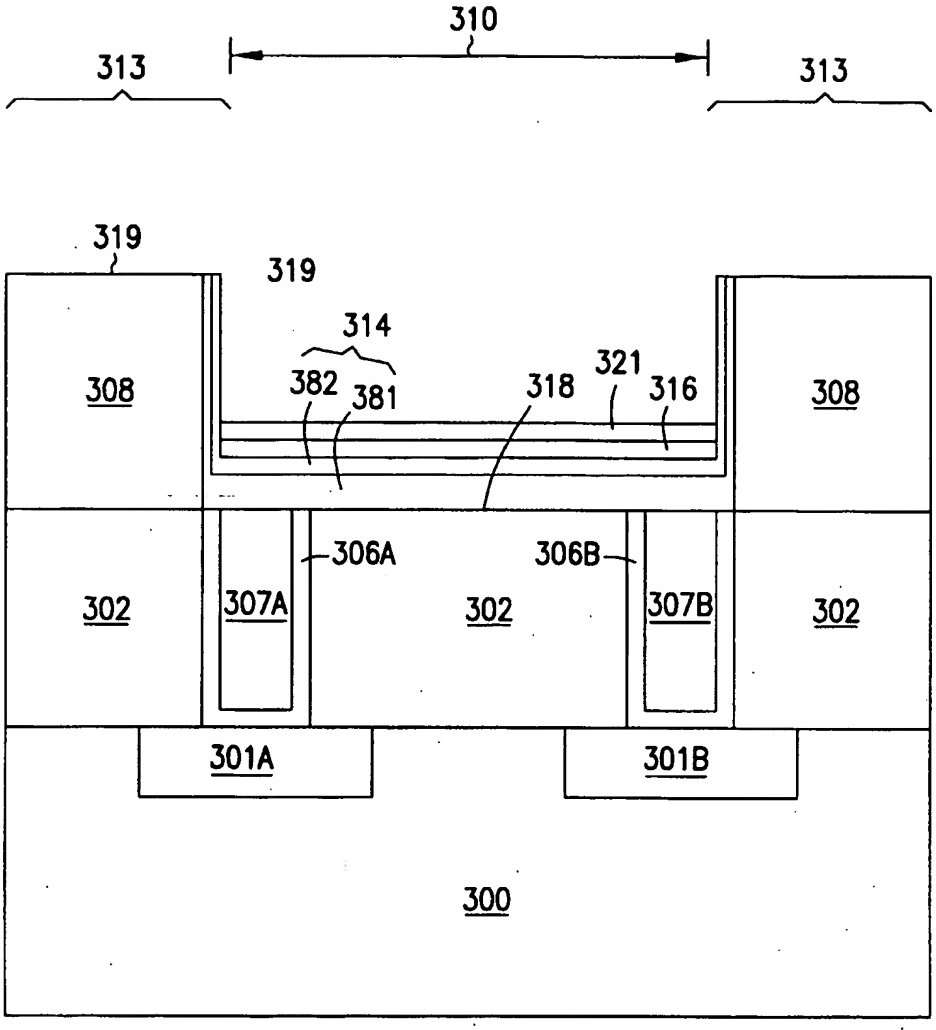
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FIG. 3E

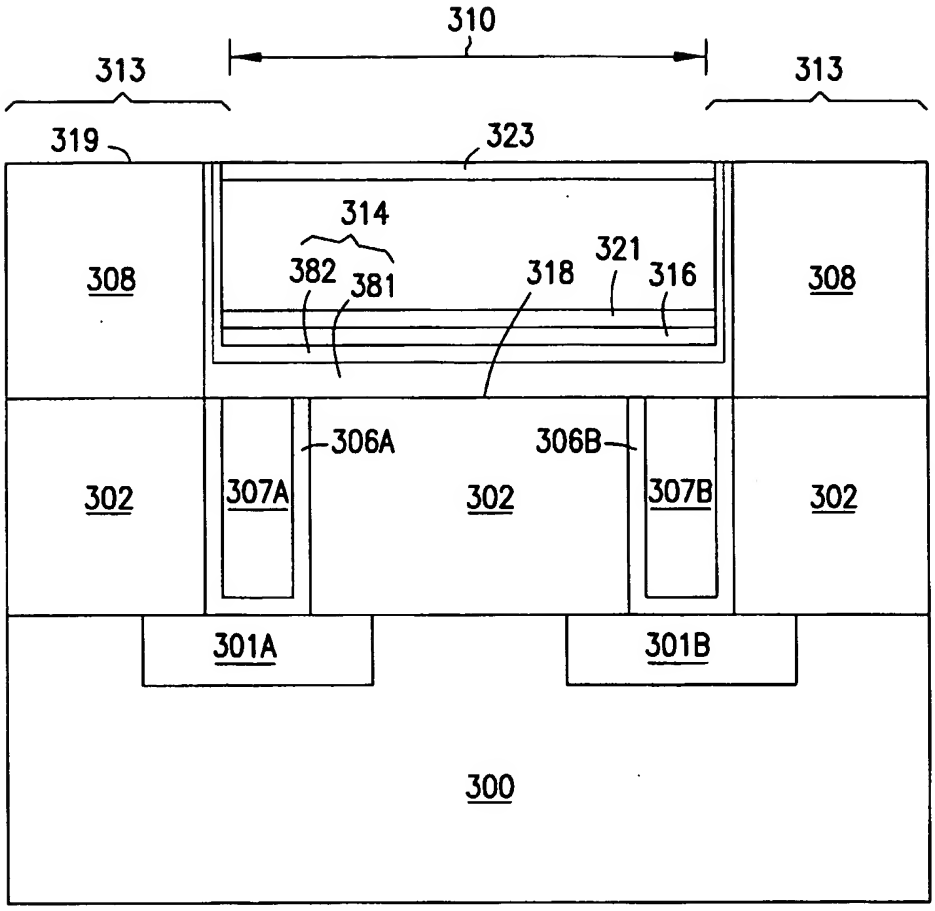
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FIG. 3F

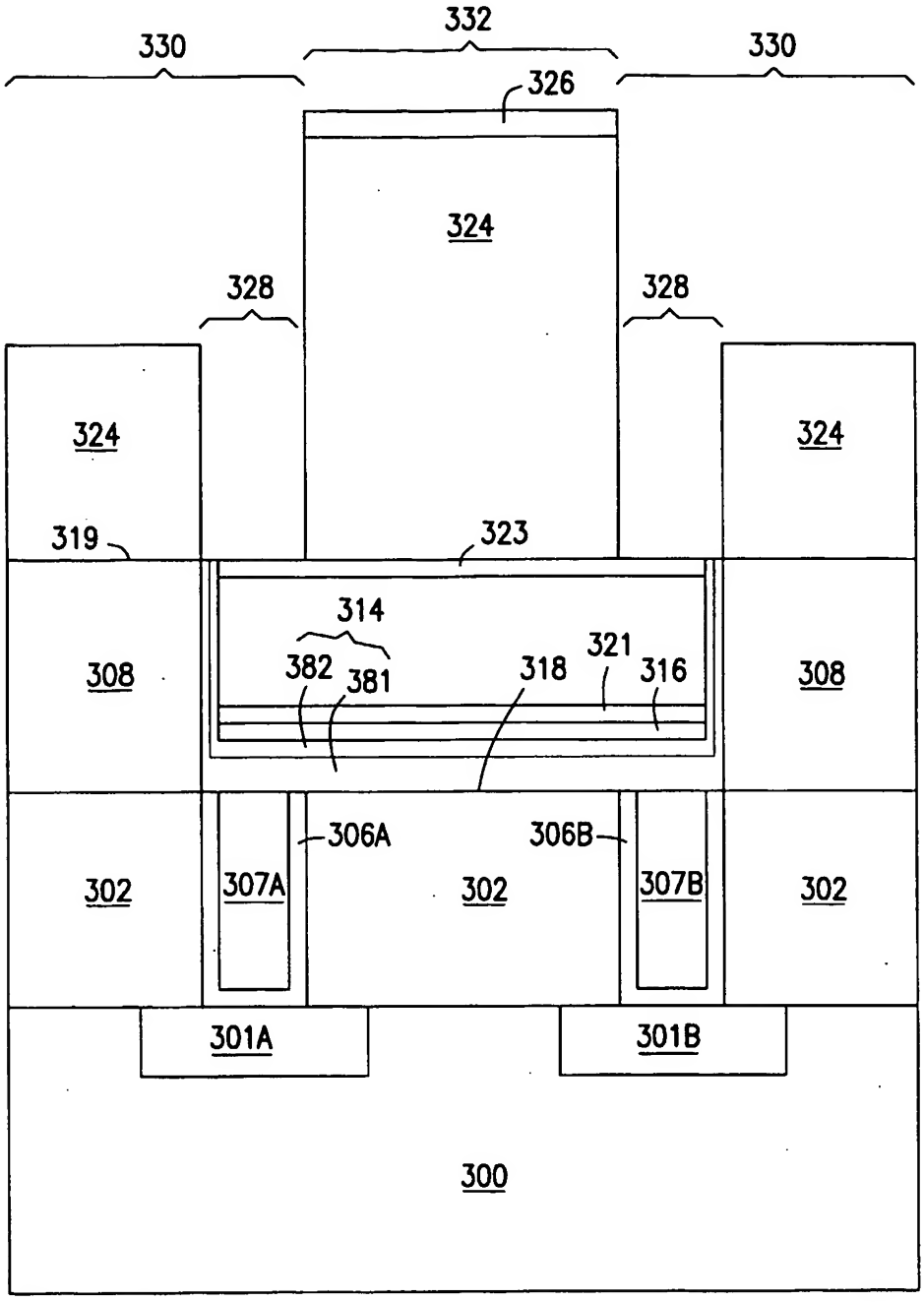
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FIG. 3G

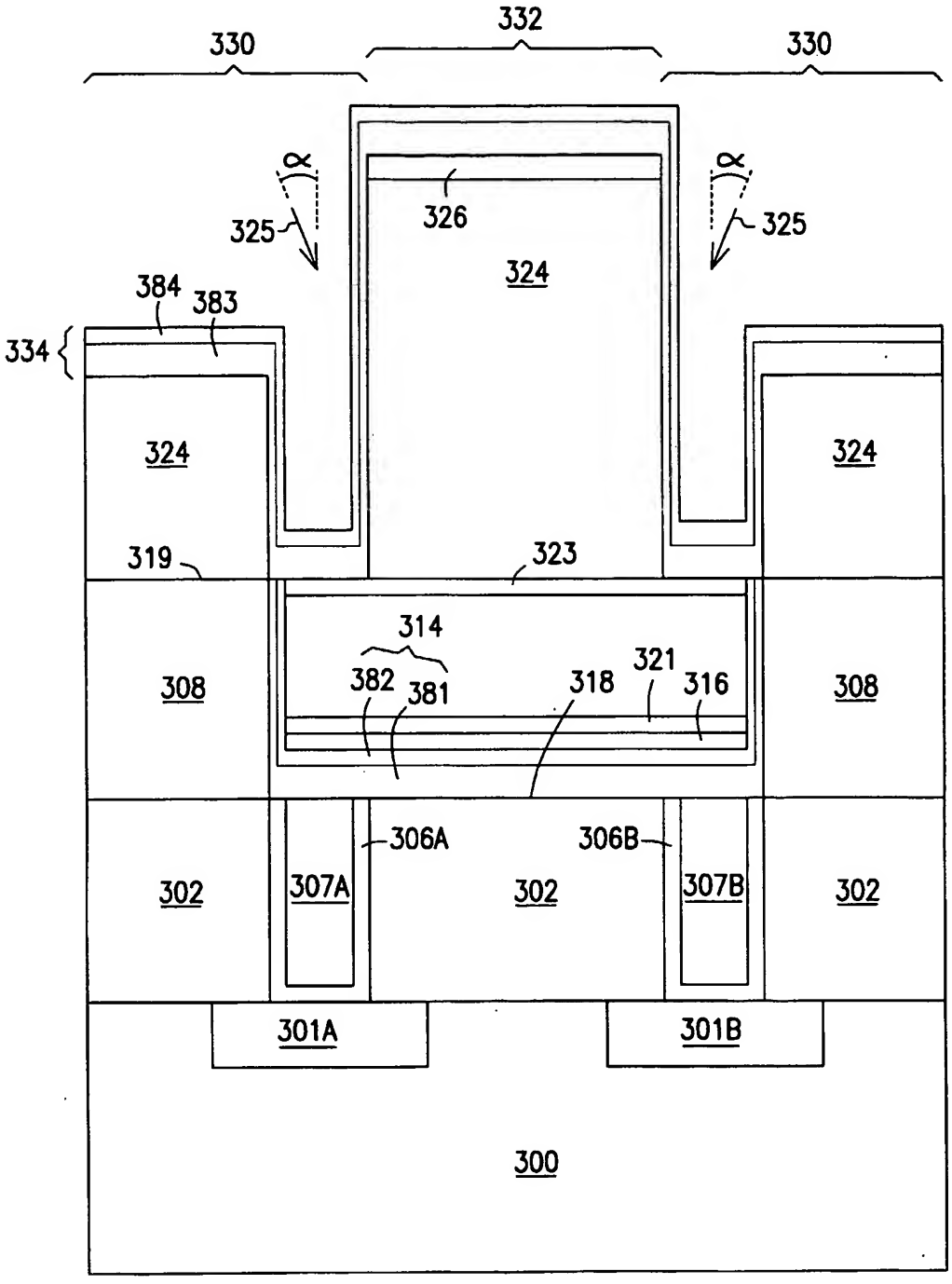
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FIG. 3H

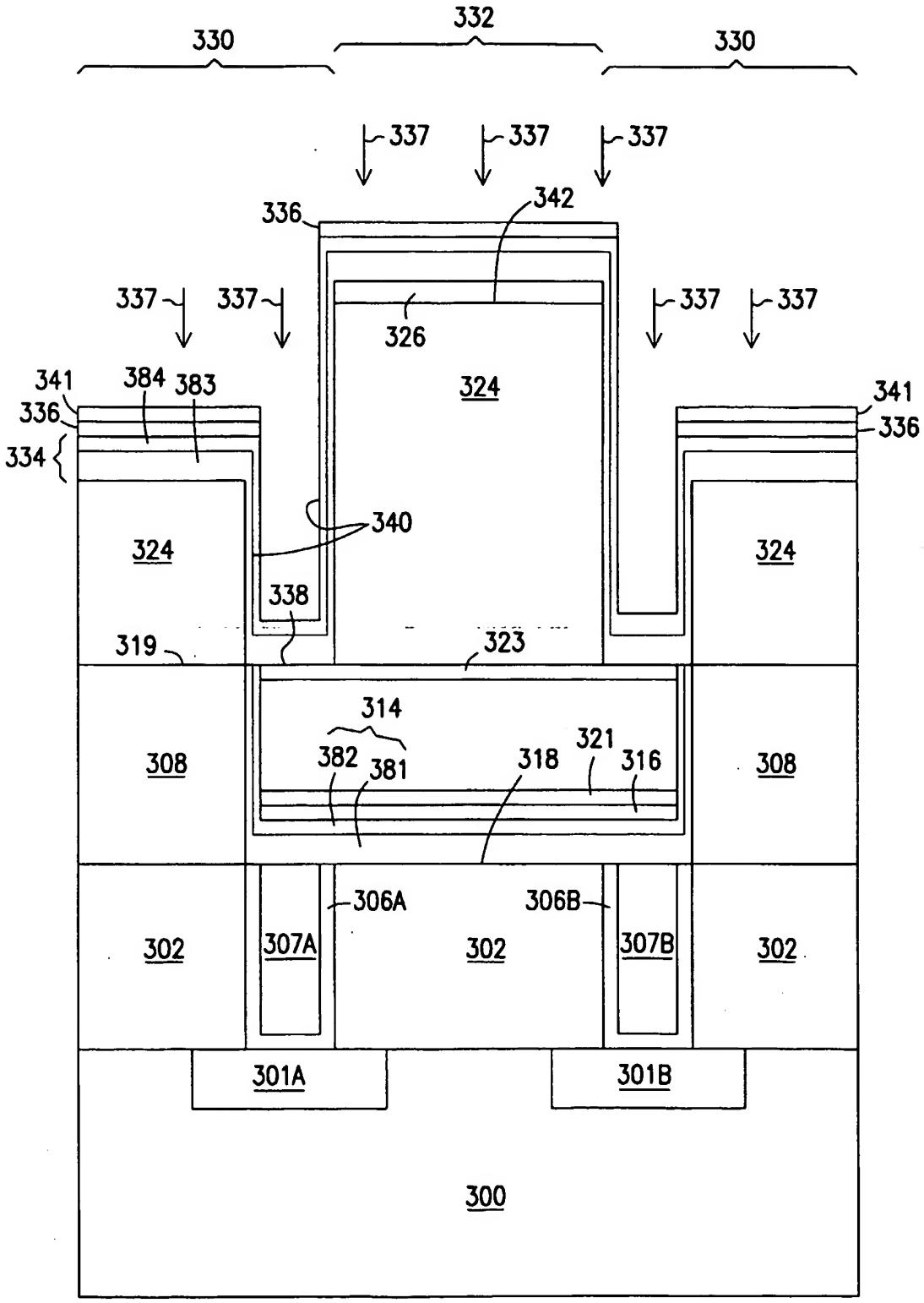
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FIG. 31

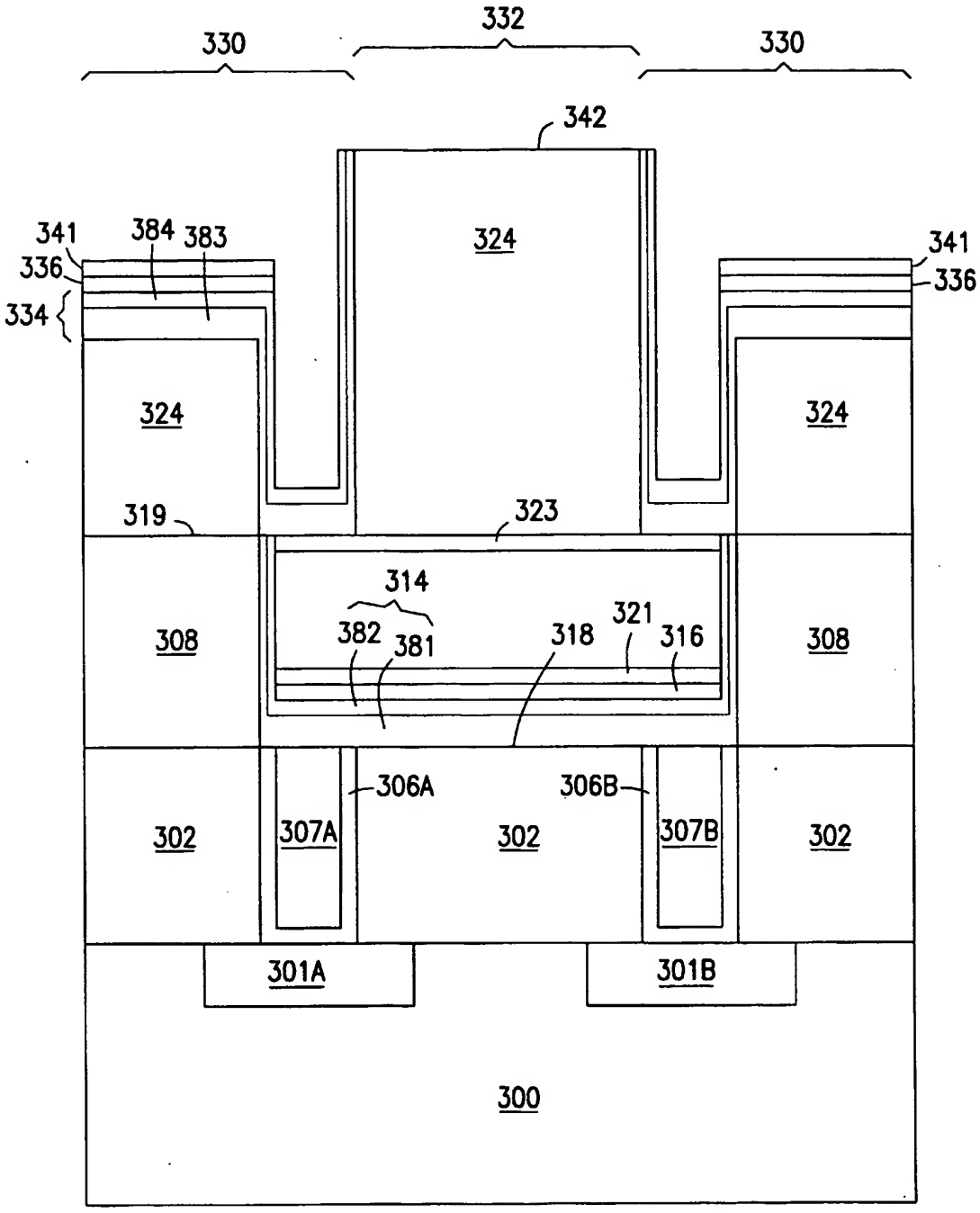
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FIG. 3J

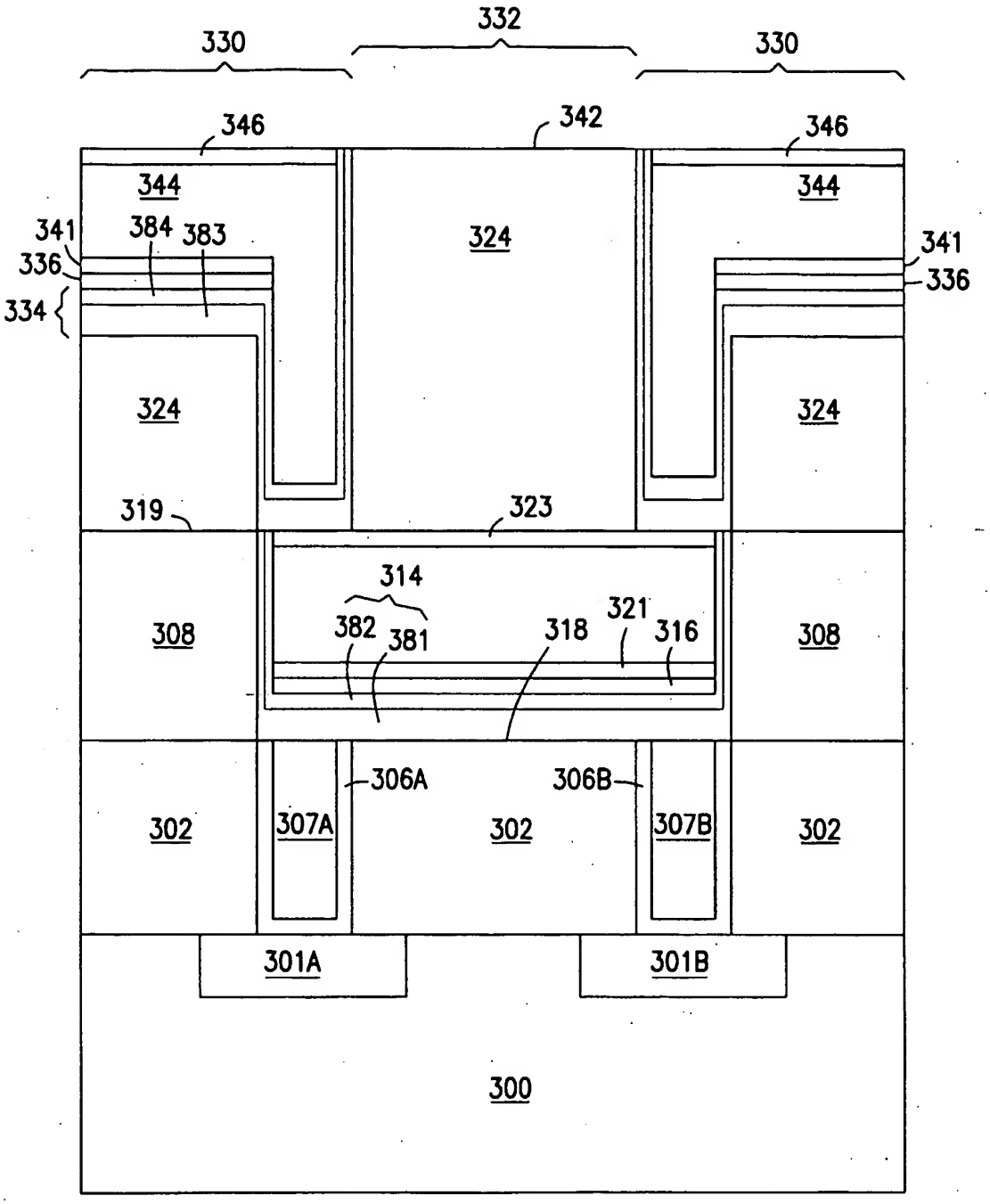
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FIG. 3K

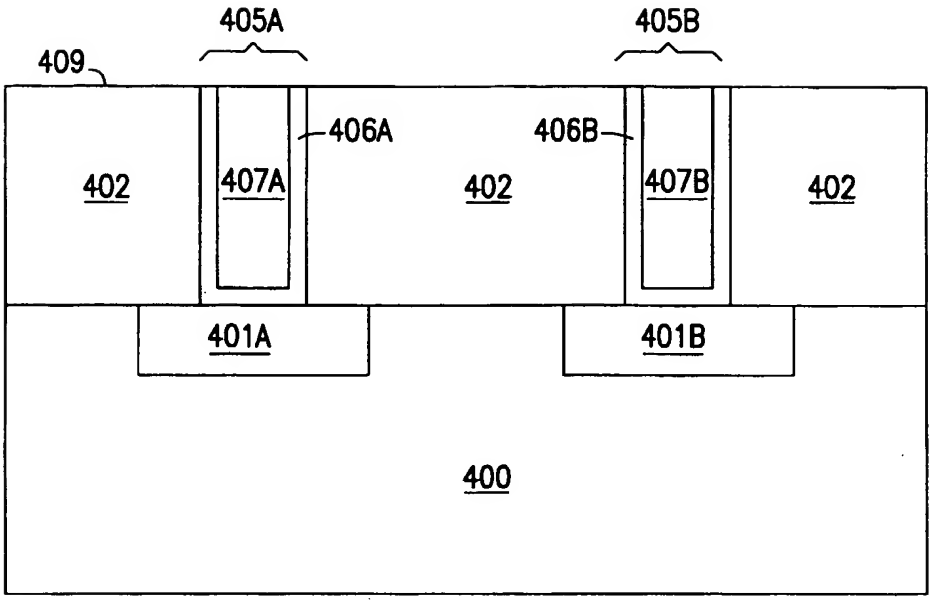

FIG. 4A

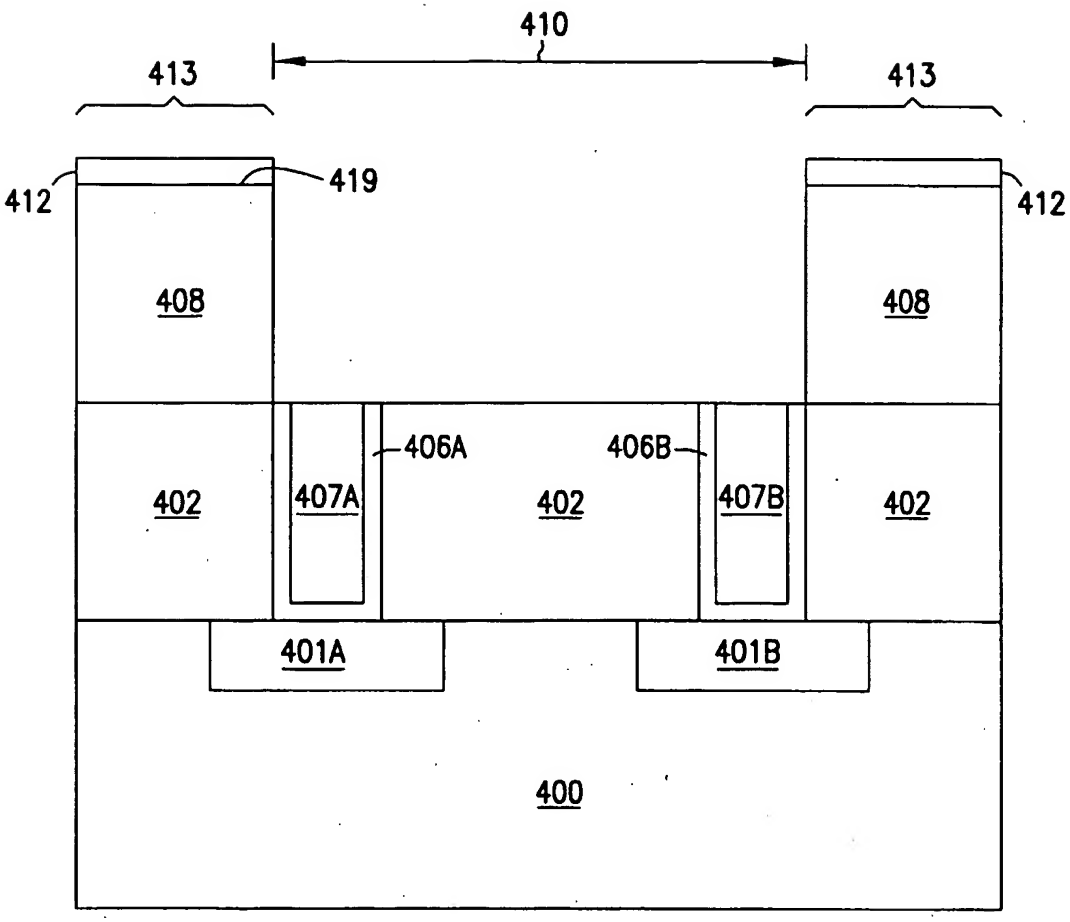
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FIG. 4B

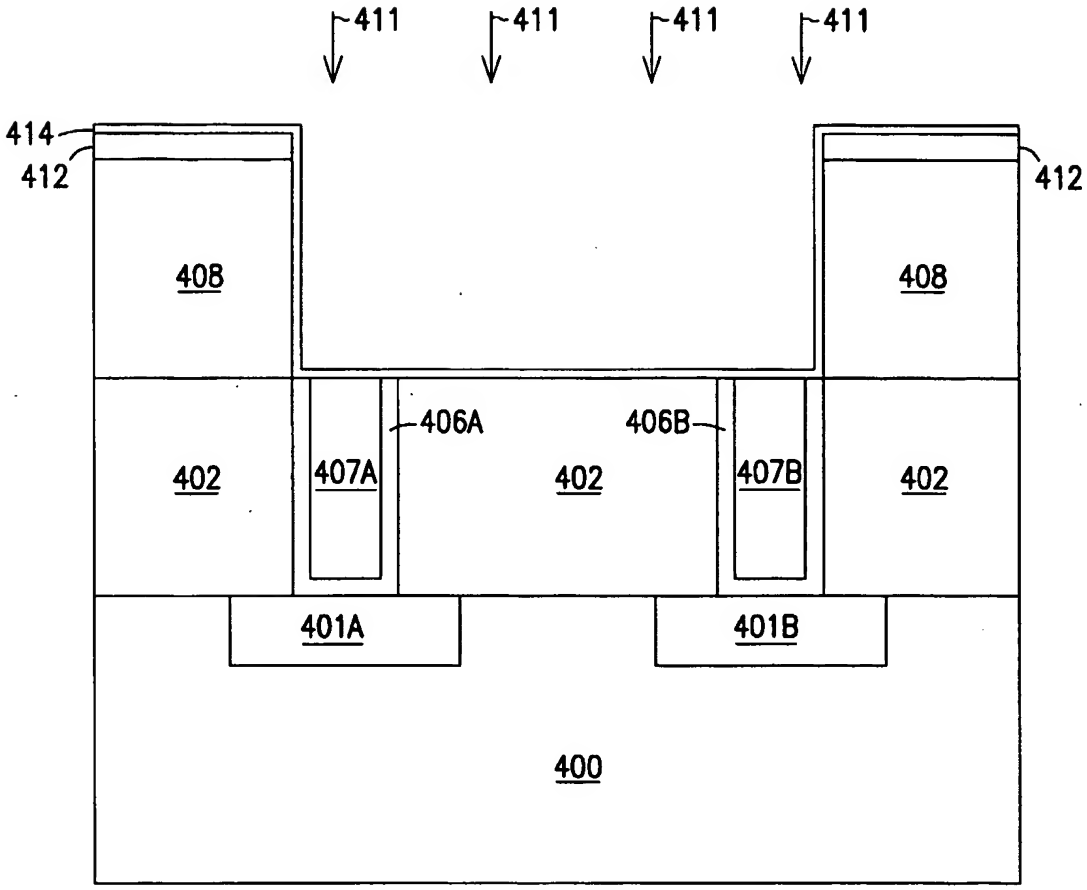
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FIG. 4C

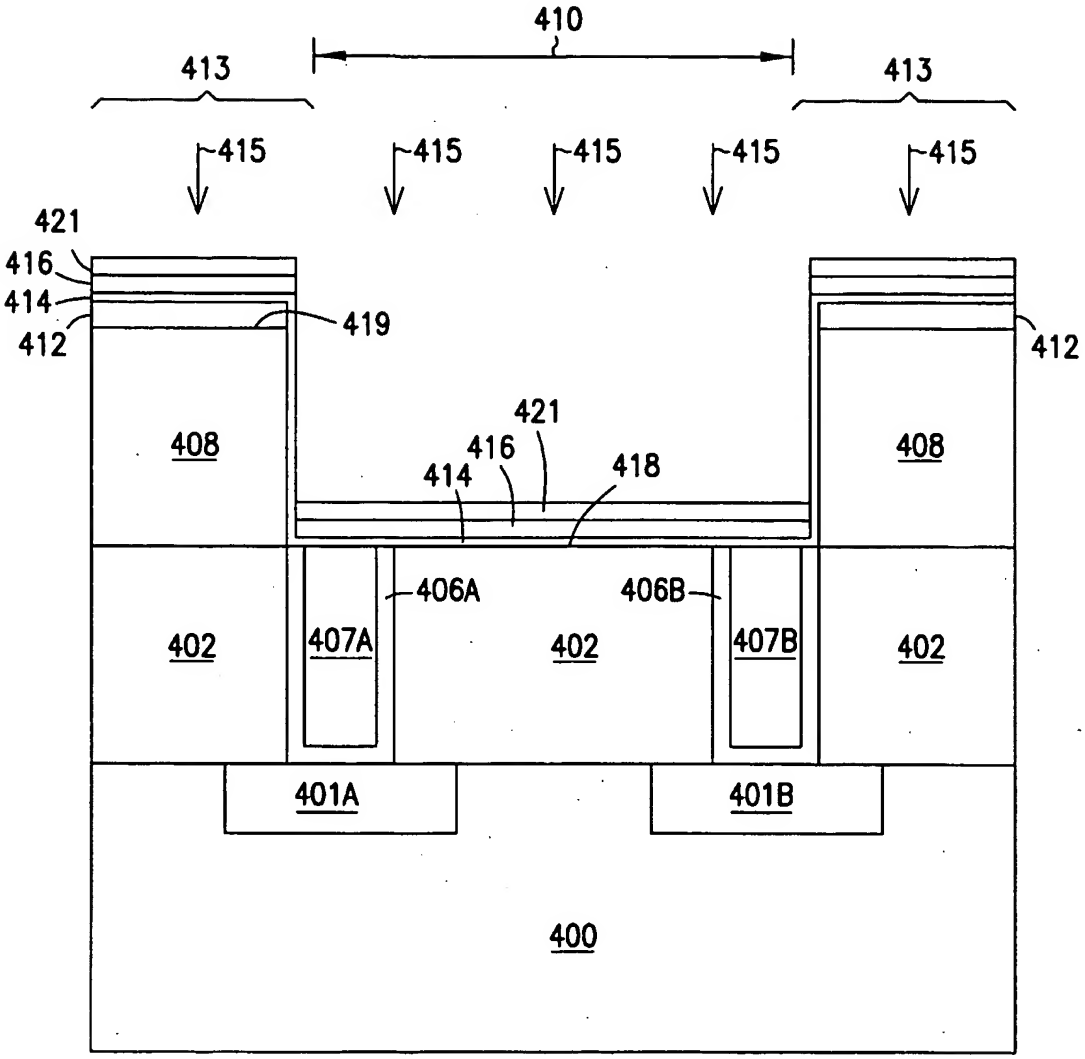
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FIG. 4D

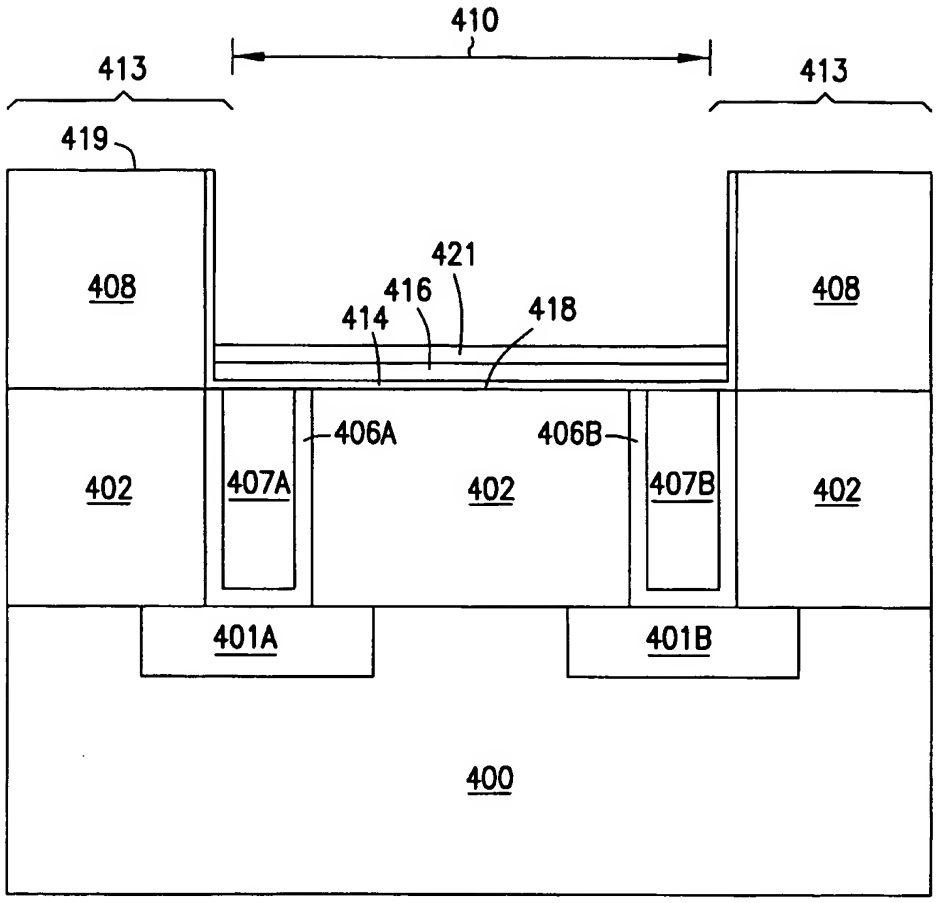
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FIG. 4E

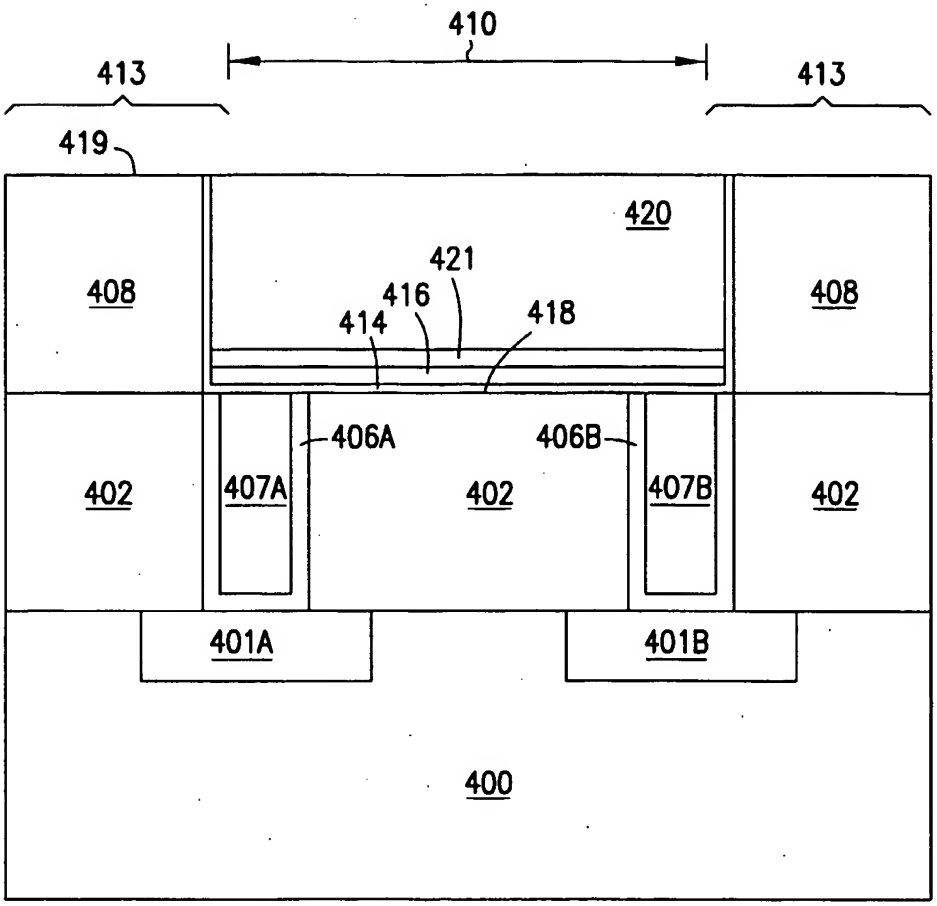
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FIG. 4F

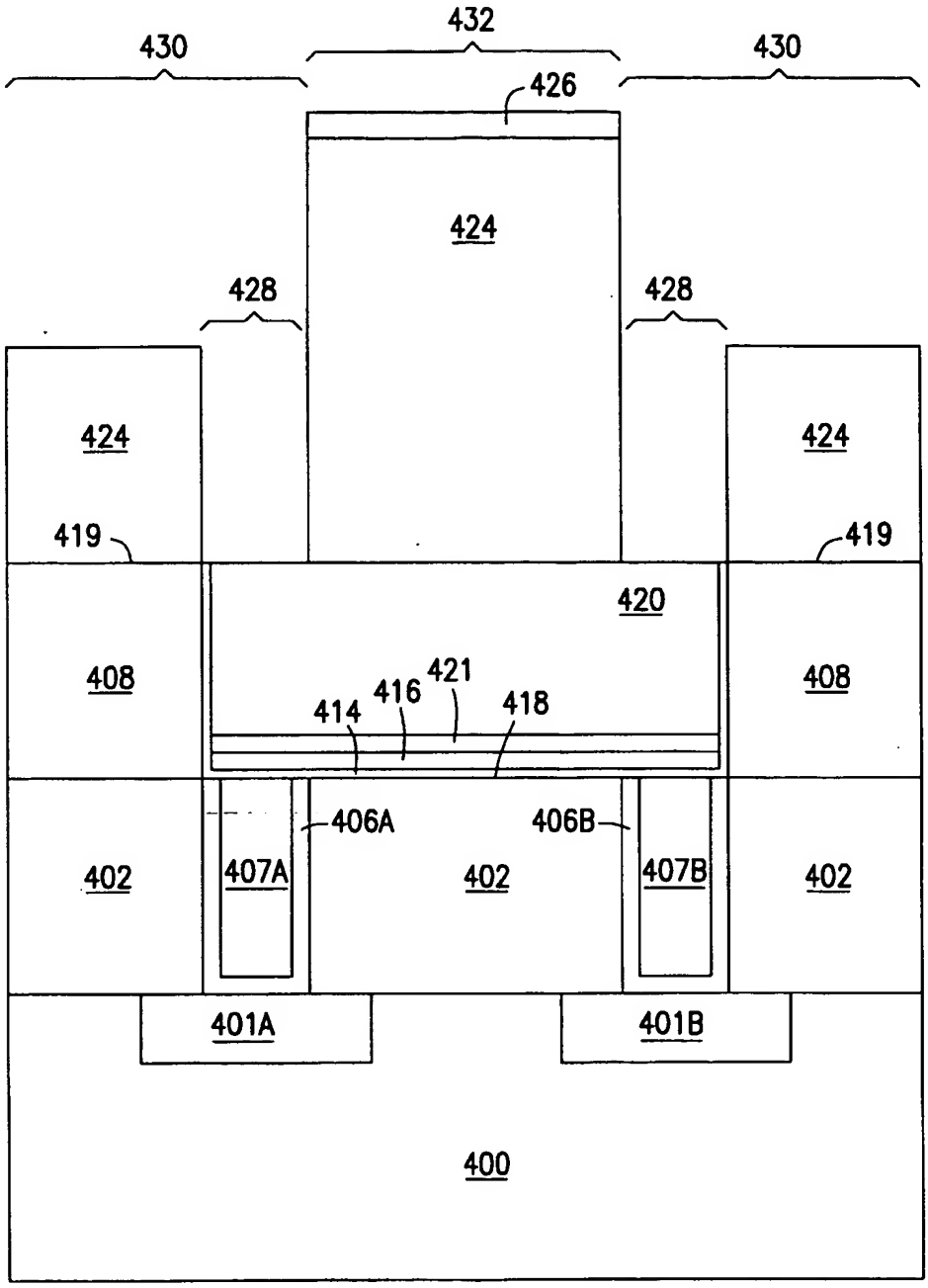
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FIG. 4G

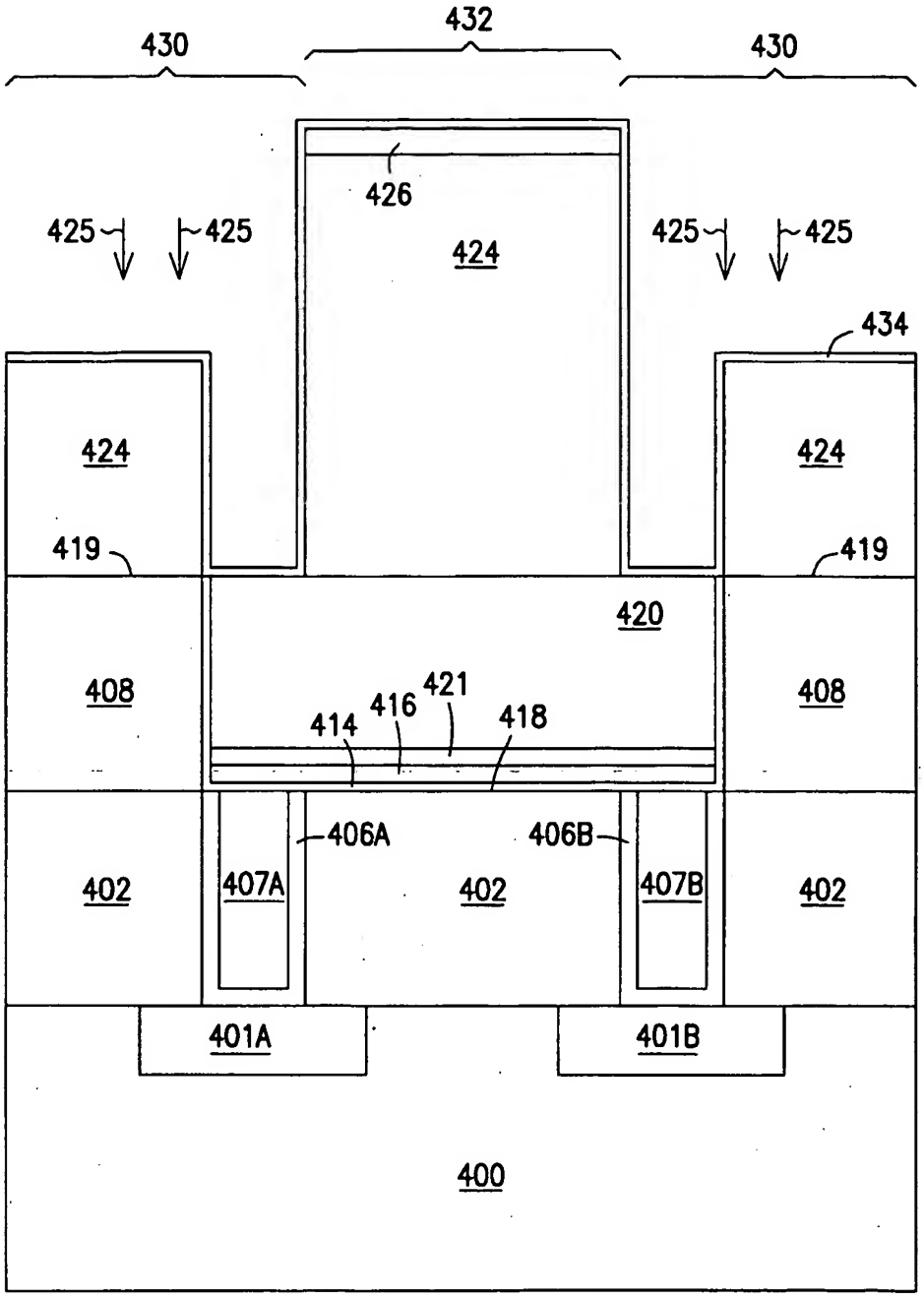
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FIG. 4H

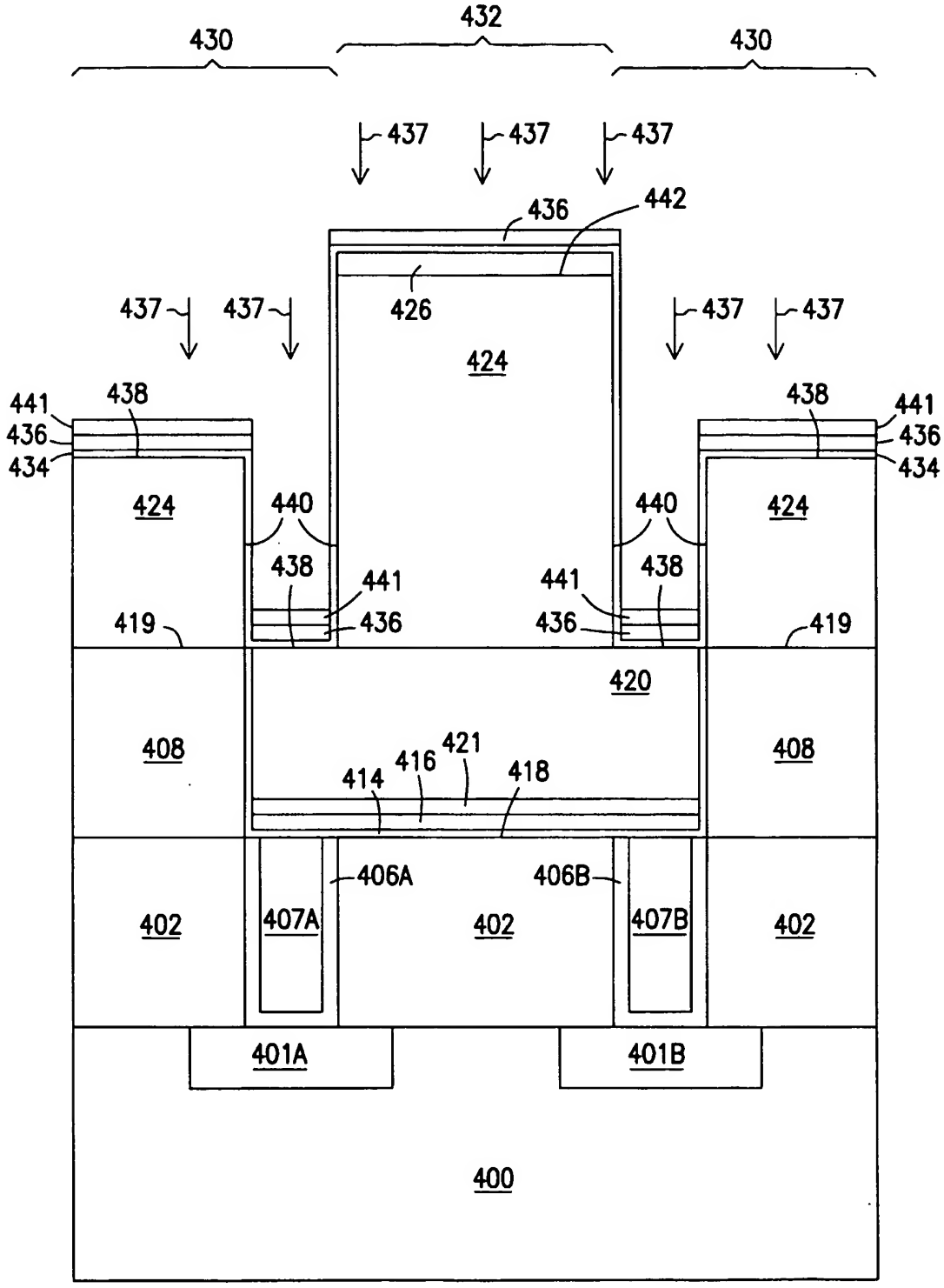
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FIG. 41

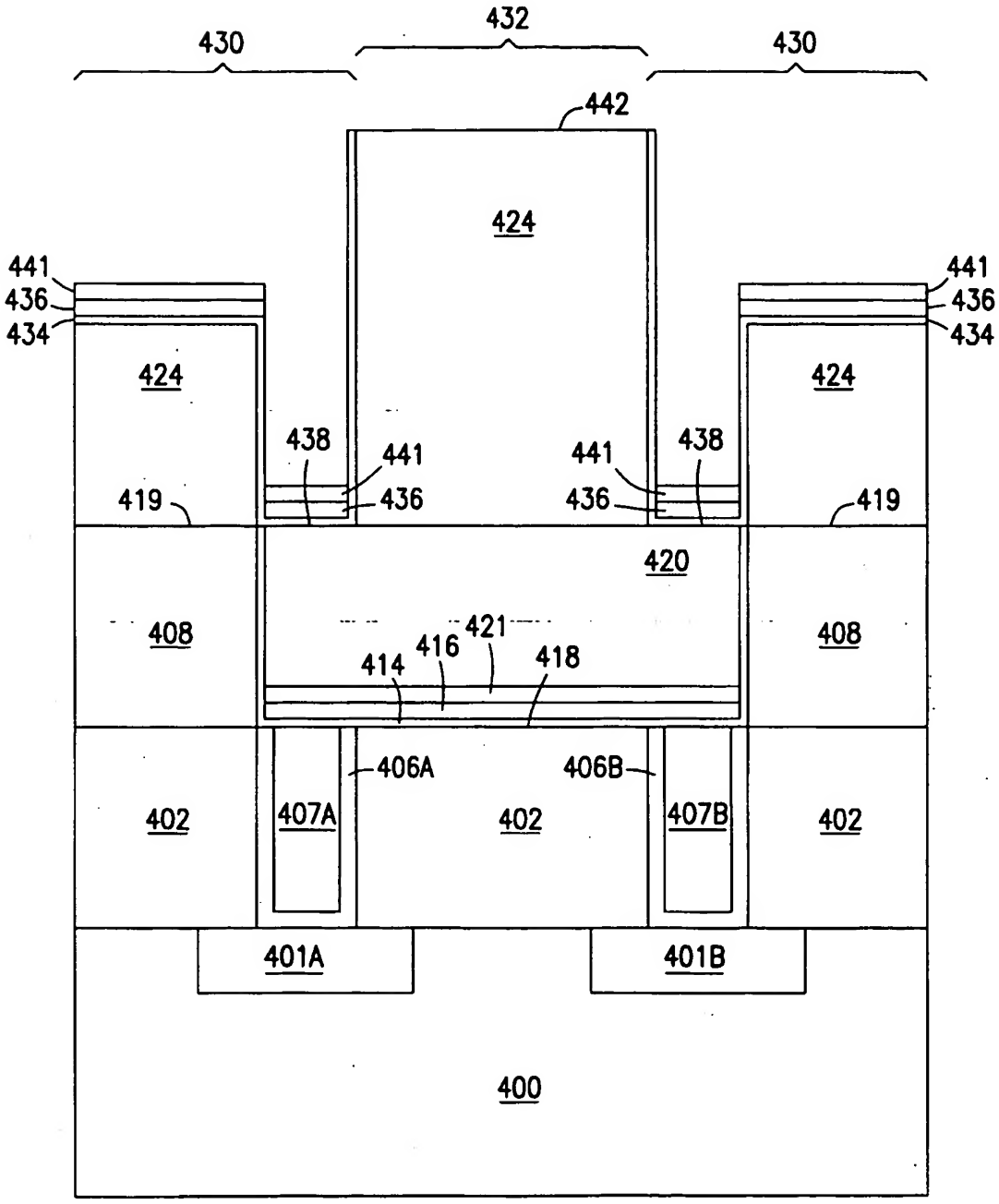
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FIG. 4J

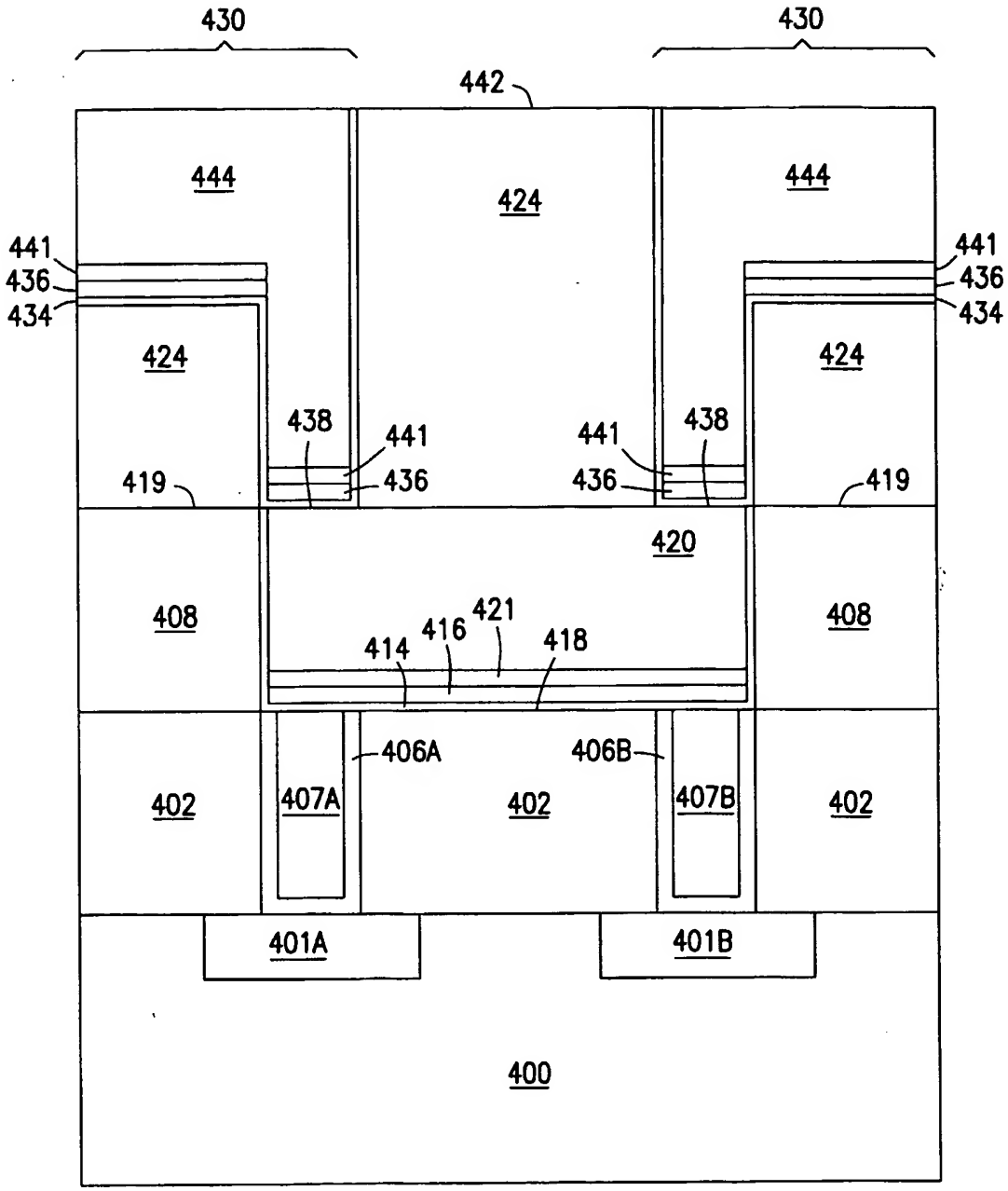
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FIG. 4K

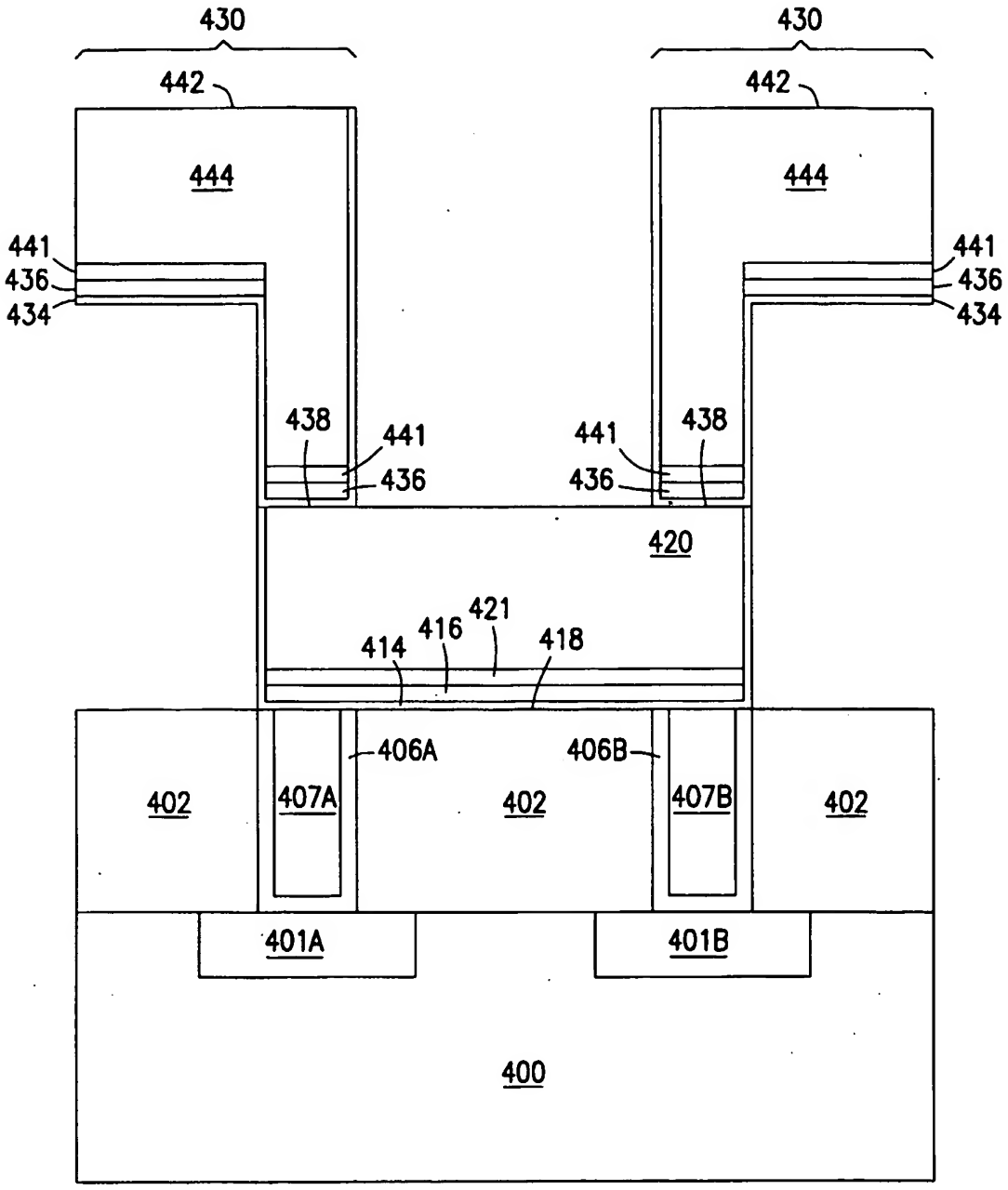
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FIG. 4L

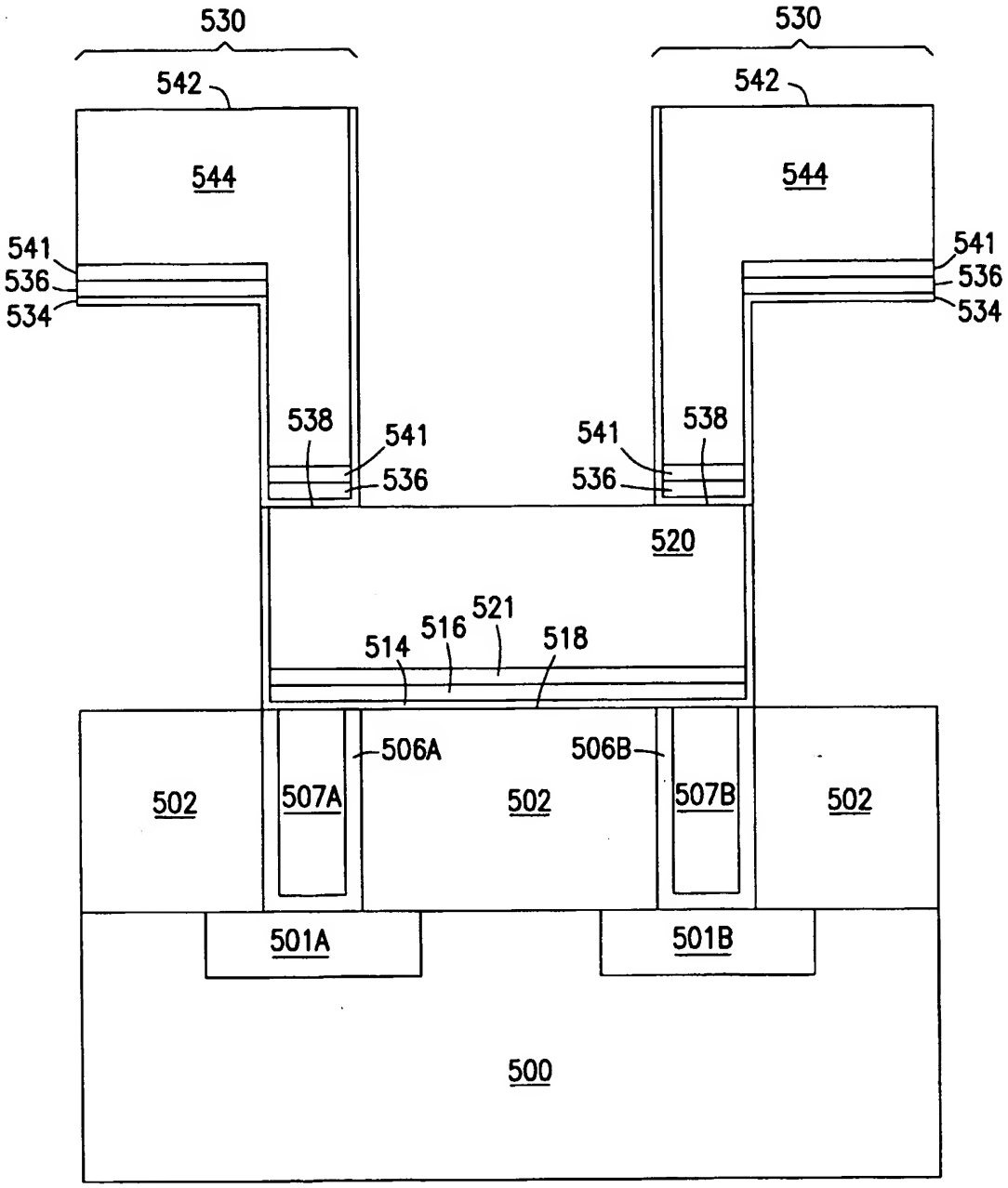
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FIG. 5

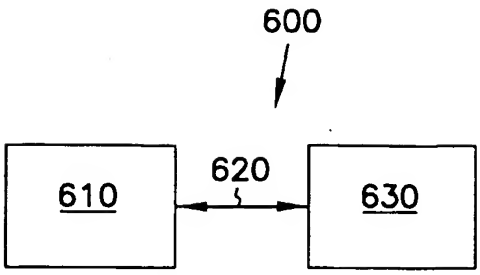

FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/01634

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	STROUD P T: "Preferential deposition of silver induced by low energy gold ion implantation" THIN SOLID FILMS, FEB. 1972, SWITZERLAND, vol. 9, no. 2, pages 273-281, XP000993098 ISSN: 0040-6090 abstract page 273, paragraph 2 -page 274, paragraph 4 page 276; figure 2 --- -/--	1-69

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 April 2001	14/05/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Micke, K

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 06, 31 July 1995 (1995-07-31) -& JP 07 078815 A (KAWASAKI STEEL CORP), 20 March 1995 (1995-03-20) abstract column 2, paragraph 9 -column 4, paragraph 15; figure 1	1-69
A	US 5 654 245 A (ALLEN GREGORY LEE) 5 August 1997 (1997-08-05) column 5, line 21 - line 51 column 7, line 8 - line 21; figures 5,6	1-69
A	US 5 670 420 A (CHOI KYEONG KEUN) 23 September 1997 (1997-09-23) the whole document	1-69
A	BHASALI S ET AL: "A NOVEL TECHNIQUE FOR FABRICATION OF METALLIC STRUCTURES ON POLYIMIDE BY SELECTIVE ELECTROLESS COPPER PLATING USING ION IMPLANTATION" THIN SOLID FILMS,CH,ELSEVIER-SEQUOIA S.A. LAUSANNE, vol. 270, no. 1/02, 1 December 1995 (1995-12-01), pages 489-492, XP000595256 ISSN: 0040-6090 the whole document	1-69
A	SHACHAM-DIAMAND Y ET AL: "Copper electroless deposition technology for ultra-large-scale-integration (ULSI) metallization" MICROELECTRONIC ENGINEERING,NL,ELSEVIER PUBLISHERS BV., AMSTERDAM, vol. 33, no. 1, 1997, pages 47-58, XP004054497 ISSN: 0167-9317 cited in the application page 50, paragraph 4 -page 51, paragraph 5; figure 1	1-69

INTERNATIONAL SEARCH REPORT

Information on patent family members

national Application No
PCT/US 01/01634

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 07078815 A	20-03-1995	NONE	
US 5654245 A	05-08-1997	JP 7007078 A	10-01-1995
US 5670420 A	23-09-1997	KR 144085 B	17-08-1998

and 101B are formed in the substrate 100. An insulator layer 102 is deposited over the number of semiconductors 101A and 101B. The deposition of the insulator layer 102 can include depositing a layer of Si_3N_4 having a thickness in the range of 100 to 500 Angstroms (Å). This insulator layer will also serve as an additional barrier to impurities coming from subsequent processing steps. Contact holes 105A and 105B are opened to the number of device structures 101A and 101B using a photolithography technique. One of ordinary skill in the are will understand, upon reading this disclosure, the manner in which a photolithography technique can be used to create contact holes 105A and 105B. In one embodiment of the present invention a titanium silicide liner 106A and 106B is placed in the contact holes 105A and 105B, such a through a process such as chemical vapor deposition (CVD). Next, tungsten vias 107A and 107B can be deposited in the contact holes 105A and 105B. The tungsten vias 107A and 107B can be deposited in the contact holes using any suitable technique such as using a CVD process. The excess tungsten is then removed from the wafer surface by chemical mechanical planarization (CMP) or other suitable processes to form a planarized surface 109.

As shown in Figure 1B, a first polymer layer 108, or first layer of polyimide 108, is deposited over the wafer surface. The first polymer layer 108 may be deposited using, for example, the process and material described in co-pending and commonly assigned application U. S. Serial No. 09/128,859, entitled "Copper Metallurgy in Integrated Circuits," which is hereby incorporated by reference. In one embodiment, depositing a first polymer layer 108 includes depositing a foamed polymer layer 108. In one embodiment, the first layer of polyimide 108 is deposited and cured, forming a 5000 Å thick layer of polymer 108 after curing. As one of ordinary skill in the art will understand, upon reading this disclosure, other suitable thickness for the first layer of polyimide 108, or insulator layer/material 108, may also be deposited as suited for forming a first level metal pattern, the invention is not so limited. The first layer of polyimide 108, or first insulator layer/material 108 is patterned to define a number of trenches 110 in the first insulator layer 108 opening to a number of first level vias, e.g. tungsten vias 107A and 107B in planarized surface 109. In other words, a first level metal pattern 110 is defined in a mask layer of